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POWER EQUALIZATION OF PARALLEL CONVERTERS VIA DROOP CONTROL FOR BATTERY CHARGING

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POWER EQUALIZATION OF PARALLEL CONVERTERS VIA DROOP CONTROL FOR BATTERY CHARGING

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João Martins Junior

POWER EQUALIZATION OF PARALLEL CONVERTERS VIA DROOP CONTROL FOR BATTERY CHARGING

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Mestre em Engenharia Elétrica.

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Este trabalho é dedicado aos meus pais, à minha irmã e
à minha namorada.

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"Nada é mais digno de nosso patrocínio que o fomento da ciência e literatura.
O conhecimento é, em todo e qualquer país, a base mais segura da felicidade pública."
(George Washington, 1790)

RESUMO

A presente dissertação de mestrado desenvolve um modelo de equipamento capaz de transferir energia de um banco de baterias estacionário para um banco de baterias de um veículo elétrico. Para tal finalidade, utiliza-se o conversor Buck-Boost Não-Inversor. Esta topologia foi escolhida por apresentar saída não inversora de tensão e, devido aos níveis de tensão que os bancos de bateria excursionam, o conversor deve operar como abaixador ou elevador. Por meio da técnica de *interleaving*, são apresentados os benefícios resultantes da conexão de conversores em paralelo. Para equalização das correntes entre módulos, a técnica de controle por *droop* é utilizada, juntamente com resistores virtuais, que são resistências inseridas através da malha de controle sem dissipação de energia. Em outras palavras, sem influenciar na eficiência do conversor. Dessa forma, são apresentados o equacionamento do conversor, seu modelo dinâmico e seu regime de operação. A partir disso, dimensiona-se dois conversores de 30 kW, dos quais resultados experimentais foram extraídos. Na sequência, o conversor apresentou bom desempenho para os níveis de tensões desejados. Então, foram validados os modelos teóricos de resistências virtuais. Finalmente, o controle por *droop* foi implementado, o que demonstrou resultados satisfatórios.

Palavras-Chave: Buck-Boost Não-Inversor. Resistências Virtuais. Controle por *Droop*. Baterias de Lítio. Veículos Elétricos. PWM.

RESUMO EXPANDIDO

Introdução

Inicialmente, esta dissertação expõe dados sobre o cenário global e brasileiro relacionado a fontes de energia e a representatividade desta no setor de transporte. Dessa forma, projeções da frota de veículos elétricos e híbridos, incentivadas por políticas públicas, são apresentadas como uma maneira de reduzir a quantidade de gases de efeito estufa. Neste contexto, o laboratório Fotovoltaica da Universidade Federal de Santa Catarina (UFSC) tem, dentre seus projetos, estudos relacionados à mobilidade urbana, a exemplo de um ônibus elétrico que opera no local. Para fomentar as políticas de mobilidade em um modelo sustentável e viável economicamente e socialmente, o trabalho desenvolvido propõe a arquitetura de uma estação de carregamento para o ônibus elétrico. Desenvolve-se, então, um banco estacionário de baterias para aumentar a autonomia do veículo.

Objetivos

O objetivo geral deste trabalho é projetar um conversor CC-CC para ser aplicado a uma estação de carregamento do ônibus elétrico do laboratório Fotovoltaica. Para alcançar tal proposta, estudos sobre operação de baterias foram realizados. Ademais, os principais objetivos específicos são: estudo de conversores utilizados no carregamento de baterias capazes de operar nos limites específicos do sistema; estudo e equacionamento do conversor; dimensionamento e implementação da topologia. Outro objetivo a ser alcançado é a contribuição nos estudos de paralelismos de conversores utilizando técnicas de *Droop*.

Metodologia

Primeiramente, esta dissertação contextualiza a utilização das baterias de lítio e sua utilização em veículos elétricos. Logo, realiza-se uma revisão sobre conversores utilizados para fazer o carregamento de baterias, bem como características elétricas das baterias de lítio e suas estratégias de carregamento. Em sequência, o conversor Buck-Boost Não-Inversor é exibido e diferentes técnicas de modulação são apresentadas para operar o conversor. Dentre elas, é selecionada a técnica de modulação que permite que o conversor opere com as chaves independentes e tenha menores perdas e menores esforços nos semicondutores. Assim, é realizado um estudo para permitir o dimensionamento de dois módulos de 30 kW, que pode operar entre 520 V e 730 V, tanto na entrada como na saída. Então, é extraído seu modelo dinâmico, permitindo a implementação de resistências virtuais para realizar o controle por *Droop*.

Resultados e Discussão

O controle por droop utiliza resistências virtuais e permite a equalização de potência entre módulos, sem a necessidade de comunicação. Técnicas de intercalamento de conversores possibilitam a redução de esforços de correntes nos filtros passivos do

sistema e o aumento da frequência total vista por eles, o que possibilita a redução de seu volume. Por último, o conversor Buck-Boost Não-Inversor demonstra resultados satisfatórios, com a técnica de controle utilizada, para equalização de potência entre os módulos. Também foi verificado o efeito do desbalanceamento de correntes utilizando diferentes resistências virtuais.

Considerações finais

Neste trabalho, foi apresentado um estudo de paralelismo de conversores por meio de técnicas de intercalamento combinadas com controle por droop. O objetivo era, através da arquitetura proposta, melhorar o desempenho do veículo elétrico frente às necessidades do sistema com o desenvolvimento de um carregador CC-CC. Apesar da técnica de droop ser facilmente implementada, poucos estudos com resultados experimentais são encontrados na literatura. Futuros trabalhos sobre este modelo podem possibilitar o incremento da potência do conversor e a redução de seu tamanho, com a utilização de módulos de semicondutores encontrados no mercado e um estudo de sua eficiência global.

Palavras-chave: Buck-Boost Não-Inversor. Resistências Virtuais. Controle por *Droop*. Baterias de Lítio. Veículos Elétricos. PWM.

ABSTRACT

This master's thesis develops a model of equipment capable of transferring energy from a stationary battery bank to an electric vehicle battery bank. For this purpose, the Non-Inverting Buck-Boost converter is used. This topology was chosen because it has a non-inverting voltage output and, due to the voltage levels that the battery banks travel, the converter must operate as a stepper-down or stepper-up. Through the interleaving technique, the benefits resulting from connecting parallel converters are presented. For electrical current equalization between modules, the droop control technique is used, together with virtual resistors, which are resistors inserted through the control loop without energy dissipation. In other words, without influencing the converter's efficiency. In this way, the equation of the converter, its dynamic model, and its operating regime are presented. From that, two 30 kW converters are dimensioned, from which experimental results were extracted. In sequence, the converter performed well for the desired voltage levels. Then, the theoretical models of virtual resistances were validated. Finally, control by droop was implemented, which demonstrated satisfactory results.

Keywords: Non-Inverting Buck-Boost. Virtual Resistances. Droop Control. Lithium Batteries. Electrical Vehicles. PWM.

LIST OF FIGURES

Figure 1.1 – Brazilian Electrical Generation Matrix in TWh 21
Figure 1.2 – Evolution of Losses in the Brazilian Electricity Sector 21
Figure 1.3 – Off-Grid Electrical Vehicle Charging Station Powered by Solar Energy 23
Figure 2.1 – 15 Ah Battery Capacity according to its C-rate Curve 25
Figure 2.2 – Equivalent electrical circuit of a battery 26
Figure 2.3 – State of Charge (SoC) vs Voltage in charge and discharge 27
Figure 2.4 – Constant Voltage - Constant Current Charging Strategy 27
Figure 2.5 – Implemented Architecture 28
Figure 2.6 – Battery Pack Internal Structure 28
Figure 2.7 – Cell voltage vs discharge capacity 29
Figure 2.8 – Cell voltage vs charge capacity 30
Figure 2.9 – Equivalent electrical circuit of a LIB 30
Figure 2.10 – Open Circuit Voltages according SOC - Computational Simulation . 32
Figure 3.1 – Phase-Shifted Full-Bridge 35
Figure 3.2 – Asymmetrical T-type Isolated Four-Level DC-DC Battery Charger . . 36
Figure 3.3 – Interleaved Buck Converter 37
Figure 3.4 – Interleaved Boost converter 37
Figure 3.5 – Interleaved Non-Inverting Buck-Boost converter 39
Figure 4.1 – Non-inverting Buck-Boost Topology 40
Figure 4.2 – Modulation signal, Carrier, and PWM Pulse 41
Figure 4.3 – Topological States of a Non-inverting Buck-Boost 42
Figure 4.4 – Converter Waveforms 43
Figure 4.5 – Buck-Boost Converter with batteries 49
Figure 4.6 – Open loop operation of the converter 49
Figure 4.7 – Current control in a close loop system 50
Figure 4.8 – Input Filter Waveforms 51
Figure 4.9 – Waveforms on output filter 53
Figure 4.10 – Two level non-inverting Buck-Boost 54
Figure 4.11 – Operation modes of two level Buck-Boost converter 54
Figure 4.12 – Input current on two level Buck-Boost 55
Figure 4.13 – Output current on two level Buck-Boost 56
Figure 4.14 – Normalized ripple voltage over input capacitor 57
Figure 4.15 – Normalized ripple current on input inductor 59
Figure 4.16 – Normalized ripple voltage at output capacitor 60
Figure 4.17 – Normalized ripple current in output inductor 61
Figure 5.1 – Buck Topology 63
Figure 5.2 – Modulation singnal, Carrier, and PWM Pulse 64

Figure 5.3 – PWM Pulses for 2 Interleaved converters 65
Figure 5.4 – Topological States of Buck Converter 65
Figure 5.5 – Buck CCM Waveforms 66
Figure 5.6 – Current ripple and Voltage ripple on the Capacitor 69
Figure 5.7 – Buck Converter with Batteries 73
Figure 5.8 – Input Filter Waveforms 74
Figure 5.9 – Two Level Buck Topology 77
Figure 5.10 – Operation Mode of Two Level Buck 77
Figure 5.11 – Output current of Two Interleaved Buck Converters 78
Figure 5.12 – Input Currents of 2 Level Interleaved Buck 79
Figure 5.13 – Interleaved Buck 80
Figure 5.14 – Ripple voltage at input capacitor 81
Figure 5.15 – Ripple current on the input inductor 83
Figure 5.16 – Ripple current at output of interleaved converters 84
Figure 5.17 – Ripple voltage at output capacitor 85
Figure 5.18 – Normalized ripple voltage at output capacitor 86
Figure 6.1 – DC Boost topology 87
Figure 6.2 – Topological States of Boost Converter 88
Figure 6.3 – Boost CCM Waveforms 89
Figure 6.4 – Boost Converter with Batteries 95
Figure 6.5 – Input capacitor current 96
Figure 6.6 – Waveforms of output filter 97
Figure 6.7 – Two level boost topology 99
Figure 6.8 – Two level boost operating mode 99
Figure 6.9 – Input current and inductor currents 100
Figure 6.10 – Diodes current and output current 101
Figure 6.11 – N-level Boost 102
Figure 6.12 – Input Current Ripple 103
Figure 6.13 – Input Capacitor Current 104
Figure 6.14 – Ripple voltage on output capacitor 106
Figure 7.1 – Ten Level NIBB structure 110
Figure 7.2 – Two Level NIBB structure 110
Figure 7.3 – Semiconductors Connection Structure 112
Figure 7.4 – Converter Thermal Model 113
Figure 7.5 – RMS Current in Input Capacitor C_i 119
Figure 7.6 – RMS Current in Output Capacitor C_o 121
Figure 7.7 – Gate Driver 122
Figure 7.8 – Control Board 123
Figure 7.9 – Perspective view of the Converter 124

Figure 7.10–Frontal view of the Converter 125
Figure 7.11–Internal view of the Converter 126
Figure 8.1 – Droop Structure 127
Figure 8.2 – Droop Structure Electrical Model 128
Figure 8.3 – Output Characteristic 1 129
Figure 8.4 – Output Characteristic 2 129
Figure 8.5 – Droop 1 130
Figure 8.6 – Droop 1 Curves 130
Figure 8.7 – Droop 2 131
Figure 8.8 – Droop 2 Curves 131
Figure 8.9 – NIBB Output Voltage Control 132
Figure 8.10–Buck with virtual resistance 132
Figure 8.11–Charging Batteries with Droop Control 133
Figure 8.12–Modified Droop Control for Constant Current Constant Voltage Charging Method 134
Figure 8.13–First topological state - Buck 139
Figure 8.14–Second topological state - Buck 141
Figure 8.15–First topological state - Boost 143
Figure 8.16–Second topological state - Boost 145
Figure 8.17–Converter Structure for Control Plant 147
Figure 8.18–Bode Diagram - Output Voltage 149
Figure 8.19–Bode Diagram - Output Current 149
Figure 8.20–Block Diagram 150
Figure 8.21–Compensated Open Loop Transfer Functions - Output Current . . . 152
Figure 9.1 – Open Loop Test Setup 154
Figure 9.2 – V_{S1} and Gate Voltage (Gate turn on) 155
Figure 9.3 – V_{S1} and Gate Voltage (Gate turn off) 156
Figure 9.4 – V_{S1} and V_{D1} - Transition Gate OFF to Gate ON 156
Figure 9.5 – V_{S1} and V_{D1} - Transition Gate ON to Gate OFF 157
Figure 9.6 – V_{S1} and $I_{L_{bb}}$ 157
Figure 9.7 – $I_{L_{bb}}$ Ripple 158
Figure 9.8 – V_{S2} and Gate Voltage (Gate turn on) 159
Figure 9.9 – V_{S2} and Gate Voltage (Gate turn off) 159
Figure 9.10–V_{S2} and V_{D2} - Transition Gate OFF to Gate ON 160
Figure 9.11–V_{S2} and V_{D2} - Transition Gate ON to Gate OFF 160
Figure 9.12–V_{S2} and $I_{L_{bb}}$ 161
Figure 9.13–$I_{L_{bb}}$ Ripple 161
Figure 9.14–Test Setup - Virtual Resistances 163
Figure 9.15–Experimental Results - Virtual Resistance in Buck Mode 164

Figure 9.16–Experimental Results - Virtual Resistance in Boost Mode 165
Figure 9.17–Test Setup - Virtual Resistances 166
Figure 9.18–Experimental Results - Droop Control 01 167
Figure 9.19–Experimental Results - Droop Control 02 168
Figure 9.20–Experimental Results - Droop Control 03 169
Figure 9.21–Experimental Results - Droop Control 04 170
Figure 9.22–Experimental Results - Droop Control 05 171
Figure 9.23–Experimental Results - Droop Control 06 172
Figure 9.24–Inductor Currents 173
Figure A.1 – Four level switching command 179

LIST OF TABLES

Table 3.1 – Power Levels for DC Charging 34
Table 7.1 – Converters Comparison 108
Table 7.2 – IGBT and Diode Parameters 115
Table 7.3 – Total Losses Per IGBT and Diode 116
Table 7.4 – Calculate Junction Temperatures 116
Table 9.1 – Inductor Verification 162
Table 9.2 – Experimental Results Data - Virtual Resistance in Buck Mode 163
Table 9.3 – Experimental Results Data - Virtual Resistance in Boost Mode 164
Table 9.4 – Experimental Results Data - Droop Control 01 166
Table 9.5 – Experimental Results Data - Droop Control 02 167
Table 9.6 – Experimental Results Data - Droop Control 03 168
Table 9.7 – Experimental Results Data - Droop Control 04 169
Table 9.8 – Experimental Results Data - Droop Control 05 170
Table 9.9 – Experimental Results Data - Droop Control 06 171
Table A.1 – Four level Analysis 180
Table A.2 – N-level Analysis 180

LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DoD	Depth of Discharge
EMI	Electromagnetic interference
IGBT	Insulated-Gate Bipolar Transistor
LIB	Lithium-Ion Battery
MME	Ministerio de Minas e Energia
NIBB	Non-Inverting Buck-Boost
PWM	Pulse Width Modulation
RMS	Root Mean Square
SAE	Society of Automotive Engineers
SoC	State of Charge
SoH	State of Health
SSM	State Space Model
TVS	Transient Voltage Supressor
UFSC	Universidade Federal de Santa Catarina

CONTENTS

1	**INTRODUCTION**	**20**
1.1	CONTEXTUALIZATION	20
1.2	OBJECTIVES	23
1.3	SCOPE OF THIS THESIS	23
2	**UTILIZATION OF LITHIUM BATTERIES IN ELECTRICAL VEHICLES**	**25**
2.1	CHARACTERIZATION OF LITHIUM-ION BATTERIES	25
2.2	BATTERY BANK MODEL	28
2.3	EQUIVALENT ELECTRICAL CIRCUIT	30
2.4	PARTIAL CONCLUSIONS	33
3	**LITERATURE REVIEW OF CONVERTERS FOR BATTERY CHARGING**	**34**
3.1	BATTERY CHARGERS TOPOLOGIES	35
3.2	PARTIAL CONCLUSIONS	39
4	**STUDY OF NON-INVERTING BUCK-BOOST CONVERTER IN CONTINUOUS CONDUCTION MODE**	**40**
4.1	MODULATION	40
4.2	TOPOLOGICAL STATES	41
4.3	WAVEFORMS	42
4.4	ALGEBRAIC ANALYSIS	44
4.4.1	**Inductor**	**44**
4.4.2	**Capacitor**	**45**
4.4.3	**Switches**	**45**
4.4.4	**Diodes**	**47**
4.5	CONVERTER OPERATION WITH BATTERIES	48
4.5.1	**Input Filter**	**50**
4.5.2	**Output Filter**	**52**
4.6	INTERLEAVING OPERATION	53
4.6.1	**Changes in the Input and Output Current**	**54**
4.6.2	**Interleaved NIBB Input filter**	**56**
4.6.3	**Interleaved NIBB Output Filter**	**59**
4.7	PARTIAL CONCLUSIONS	62
5	**STUDY OF BUCK CONVERTER IN CONTINUOUS CONDUCTION MODE**	**63**
5.1	MODULATION	63
5.2	TOPOLOGICAL STATES	65
5.3	WAVEFORMS	66
5.4	ALGEBRAIC ANALYSIS	66

5.4.1 Inductor . . . 67
5.4.2 Capacitor . . . 68
5.4.3 Switch . . . 69
5.4.4 Diode . . . 71
5.5 CONVERTER OPERATION WITH BATTERIES . . . 73
5.5.1 Buck Input Filter . . . 73
5.5.2 Output Filter . . . 76
5.6 INTERLEAVING OPERATION . . . 76
5.6.1 Changes in the Input and Output Current . . . 78
5.6.2 Interleaved Buck Input Filter . . . 79
5.6.3 Interleaved Buck Output Filter . . . 83
5.7 PARTIAL CONCLUSIONS . . . 86
6 STUDY OF BOOST CONVERTER IN CONTINUOUS CONDUCTION MODE . . . 87
6.1 MODULATION . . . 87
6.2 TOPOLOGICAL STATES . . . 87
6.3 WAVEFORMS . . . 88
6.4 ALGEBRAIC ANALYSIS . . . 89
6.4.1 Inductor . . . 90
6.4.2 Capacitor Boost . . . 91
6.4.3 Switch . . . 92
6.4.4 Diode . . . 93
6.5 CONVERTER OPERATION WITH BATTERIES . . . 94
6.5.1 Input filter . . . 95
6.5.2 Output filter . . . 97
6.6 INTERLEAVING OPERATION . . . 98
6.6.1 Changes in the Input and Output Current . . . 99
6.6.2 Interleaved Boost Input Filter . . . 102
6.6.3 Interleaved Boost Output Filter . . . 105
6.7 PARTIAL CONCLUSIONS . . . 107
7 DESIGN OF NON-INVERTING BUCK-BOOST CONVERTER . . . 108
7.1 STRUCTURE . . . 109
7.2 INPUT PARAMETERS . . . 110
7.3 SEMICONDUCTORS . . . 111
7.3.1 Losses Calculation and Junction Temperature Calculation . . . 113
7.4 INDUCTOR . . . 116
7.5 FILTER . . . 117
7.5.1 Buck Mode . . . 117
7.5.2 Boost Mode . . . 118

7.5.3 RMS Current in the Capacitors . . . 118
7.6 GATE DRIVER . . . 122
7.7 CONTROL BOARD . . . 123
7.8 TRANSDUCERS . . . 123
7.9 ASSEMBLY . . . 124
7.10 PARTIAL CONCLUSIONS . . . 126
8 DROOP CONTROL WITH VIRTUAL RESISTANCES . . . 127
8.1 DROOP CONTROL . . . 127
8.2 VIRTUAL RESISTANCES . . . 132
8.3 CONTROL STRATEGY . . . 133
8.4 DYNAMICAL MODELING . . . 135
8.4.1 State Space Model . . . 135
8.4.2 Buck Dynamic Model . . . 139
8.4.3 Boost Dynamic Model . . . 143
8.5 CONVERTER NUMERICAL PLANTS AND COMPENSATOR DESIGN 146
8.6 PARTIAL CONCLUSIONS . . . 153
9 EXPERIMENTAL RESULTS . . . 154
9.1 OPEN LOOP OPERATION . . . 154
9.1.1 Buck Operation . . . 154
9.1.2 Boost Operation . . . 158
9.1.3 Open Loop Results . . . 162
9.2 VIRTUAL RESISTANCES . . . 162
9.3 PARALLELING CONVERTERS - DROOP CONTROL . . . 165
9.4 PARTIAL CONCLUSIONS . . . 173
10 CONTRIBUTIONS AND FINAL CONSIDERATIONS . . . 174
REFERENCES . . . 176
APPENDIX A – INTERLEAVING OPERATION . . . 179
ANNEX A – INDUCTOR PROJECT CALCULATIONS . . . 181
ANNEX B – SOURCE CODE . . . 187
ANNEX C – SCHEMATICS . . . 194
ANNEX D – LIST OF COMPONENTS . . . 198

1 INTRODUCTION

This chapter aims to present the motivations for the execution of this master's thesis. To carry out the approach, it contextualizes the reader regarding the recent changes in the energy and mobility scenario. Then, it presents the objectives of the work and a brief description of the structure.

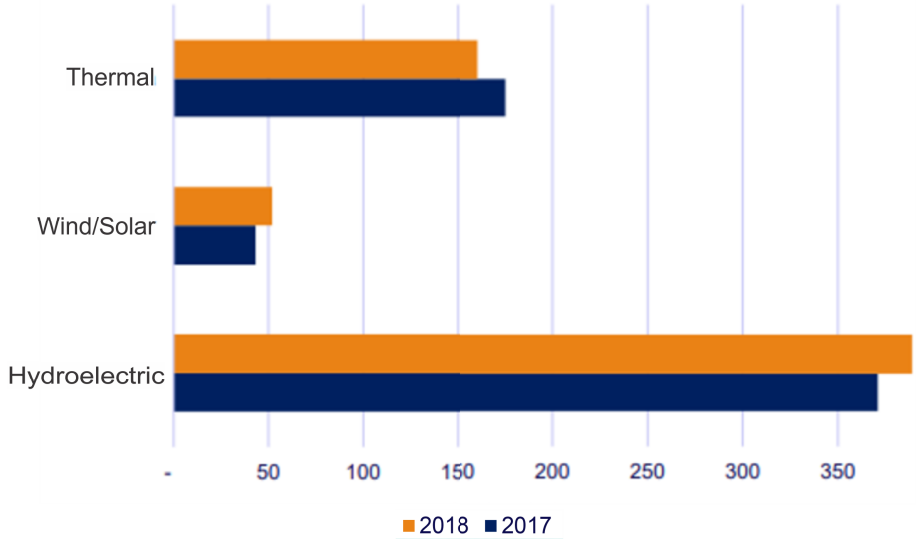
1.1 CONTEXTUALIZATION

In recent decades, the discussion about the greenhouse effect has raised concerns for society, which faces the challenge of reviewing its production systems, products, and energy matrix. A survey, released by the Energy Research Company in 2019, shows that at least 62.5% of all energy supply in Brazil comes from non-renewable thermal sources, such as oil, coal, and firewood. (MME, 2019).

The same report shows that only the transport sector held a 29% share of all energy used in Brazil. Electric and hybrid vehicles, in turn, only 0.025% of energy consumption, according to studies by the Parts Manufacturer's Union (Sindipeças). The organization's data also reveals that the fleet of electric and hybrid vehicles totals only 11,038 units, compared to the more than 44 million vehicles operating in the country (SINDIPEÇAS; ABIPEÇAS, 2019).

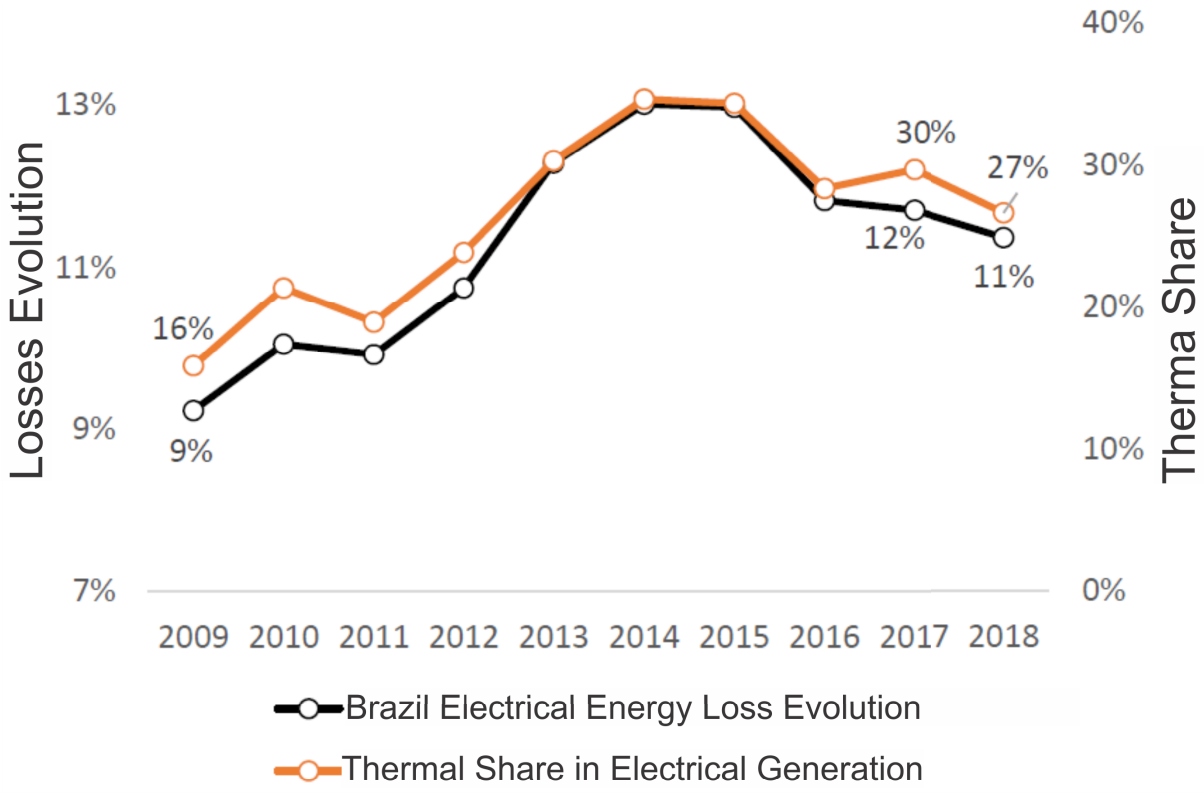
New technologies are already present to mitigate the existing problem in the release of greenhouse gases. The production of electric energy by renewable sources, such as wind and solar, are some examples. As shown in Figures 1.1 and 1.2, there was an increase in the share of these new energy sources in the Brazilian energy matrix, associated with a reduction in electricity losses.

Figure 1.1 – Brazilian Electrical Generation Matrix in TWh



Source: Adapted from (MME, 2019)

Figure 1.2 – Evolution of Losses in the Brazilian Electricity Sector



Source: Adapted from (MME, 2019)

Therefore, one of the solutions to reduce the consumption of fossil fuels is to invest in renewable energy sources. In general, the strategy generates greater efficiency

for the energy sector.

One difficulty brought about by renewable energy sources, however, is related to seasonality. This means that they cannot be dispatched, that is, these intermittent sources are subject to weather conditions.

To solve this problem, energy storage elements have been the subject of research all over the world. The proposal is to guarantee uninterrupted sources of energy in the face of variations in climatic conditions.

As a study by (ZENG et al., 2018) reveals, in an energy storage unit in South Australia, lithium batteries (with a total capacity of 100 MW - 129 MWh) were built to eliminate the intermittency generated by renewable energies. Consequently, the storage unit proved to be efficient in regulating the voltage and frequency of the electrical grid in the face of variations caused by problems with other energy sources. In this way, it solved the problem of blackouts and also forced the fall in reserve energy prices, which were monopolized by five companies (ZENG et al., 2018).

Along with the changes in the power generation system, the mobility sector has been registering an increase in the fleet of electric vehicles. According to the International Energy Agency (OUTLOOK, 2019), in 2018 approximately 5.1 million electric vehicles were sold, which represents two million more than the previous year. The same report shows an increase in the number of charging stations, with the majority being slow private chargers.

Therefore, the combination of energy generation through renewable sources and storage devices initiates a new chapter in the Electrical Current War, which occurred in the late 19th-century (NIX, 2015). With distributed generation, direct current microgrids have advantages over an alternating current, such as: greater efficiency; better integration with renewable energy sources; they are not affected by the system harmonics; and there is compensation for load fluctuation through storage elements (BARBI, 2019).

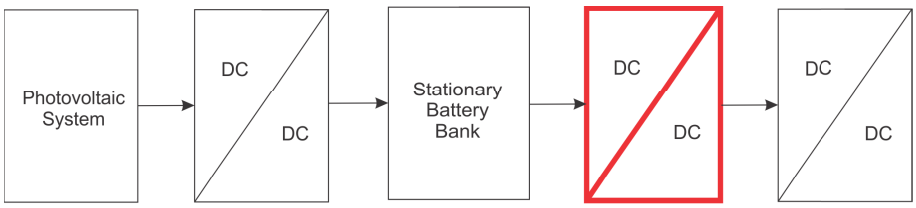
Given this trend, the Fotovoltaica Laboratory of the Federal University of Santa Catarina (UFSC) has been developing new technologies through R&D 021, financed by Engie Company, for charging electric vehicles and integrating with storage systems and the electrical power grid.

One of the objects of study for this project is the electric bus, known as the E-bus, from the Photovoltaic laboratory. Every day, the vehicle performs six round-trips, approximately 50 km each, between the university headquarters and the laboratory. The capacity of the E-bus' battery bank is enough for just one round-trip, not allowing it runs longer distances. The solution found, therefore, is to increase the autonomy of the bus.

To meet this need, this thesis discusses the development of a fast charger for the E-bus, by means of a stationary bank of lithium batteries, to be implemented at the headquarters of UFSC. This battery bank will be integrated with the photovoltaic

modules, as shown in Figure 1.3, which reduces the need for special installations to extract large amounts of energy from the power grid for short load intervals.

Figure 1.3 – Off-Grid Electrical Vehicle Charging Station Powered by Solar Energy



Source: Own Elaborated

1.2 OBJECTIVES

The general objective of this thesis is to develop a fast charger to transfer energy from a stationary battery bank to an automotive battery bank, present in the E-bus. One of the criteria for choosing the converter is the non-inversion of the output voltage.

The specific objectives of the study are:

- to define the topology to be used;
- to model, to simulate and to dimension the converter components;
- to build and to test the designed equipment.

1.3 SCOPE OF THIS THESIS

The thesis is structured in ten chapters. In the first chapter, the study's justifications and the context of the theme are presented.

The second chapter covers lithium batteries, their use, equivalent electrical model, and the design of the project to be developed.

The third chapter presents a brief review of the literature on converters used to charge lithium batteries.

The fourth, fifth, and sixth chapters show the non-inverting Buck-Boost, Buck, and Boost converters; its topologies, modulation, and equation of waveforms. The result of connecting interleaved converters is also shown.

The seventh chapter justifies the chosen converter among those presented. In sequence, it brings the dimensioning of the converter, the choice of semiconductors, and the magnetic elements.

The eighth chapter presents the dynamic model of the converter and the exposure of the virtual resistors and the slope control method.

The ninth chapter is for experimental results obtained and comparisons with theoretical values.

At last, the conclusions and final considerations obtained are made, in addition to proposals for future studies on the parallelism of converters.

2 UTILIZATION OF LITHIUM BATTERIES IN ELECTRICAL VEHICLES

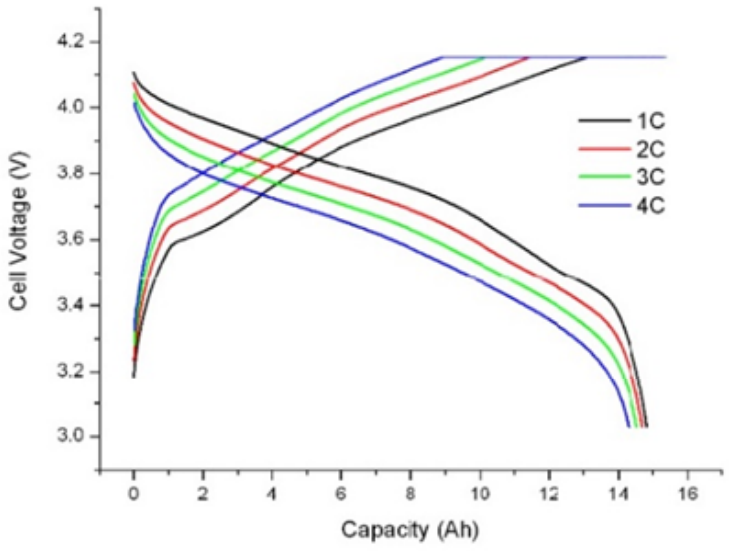
Lithium-ion batteries (LIB) have become common equipment in our daily lives. They are present in several devices that we use today, in the age of social media, such as smartphones, tablets, and notebooks. John Goodenough's first commercial model in 1991 (GOODENOUGH; MIZUCHIMA, 1981), helped to popularize portable computers, which do not require electronic wires and have long periods of autonomy.

But the use of batteries was not restricted to small devices. Today, they are used in electric vehicles, such as scooters, bicycles, cars, buses, and trucks. There is also an application in the production of renewable energy, such as energy storage units and island systems, that is, places that are not connected to the electricity grid.

2.1 CHARACTERIZATION OF LITHIUM-ION BATTERIES

One of the reasons why LIB stands out among other storage facilities is its high energy density. In other words, it is possible to store large amounts of energy in a given volume. In addition, the LIB can receive and supply high currents, has no memory effect, and also has high efficiency compared to other batteries (KIM; KWON; HYUN, 2012). It can also be characterized by its C-rate, which indicates the permitted current, given its energy storage capacity. Figure 2.1 shows a battery with a capacity of 15 Ah used by (KIM; KWON; HYUN, 2012) which can operate on region 4C, equivalent to 60 A.

Figure 2.1 – 15 Ah Battery Capacity according to its C-rate Curve



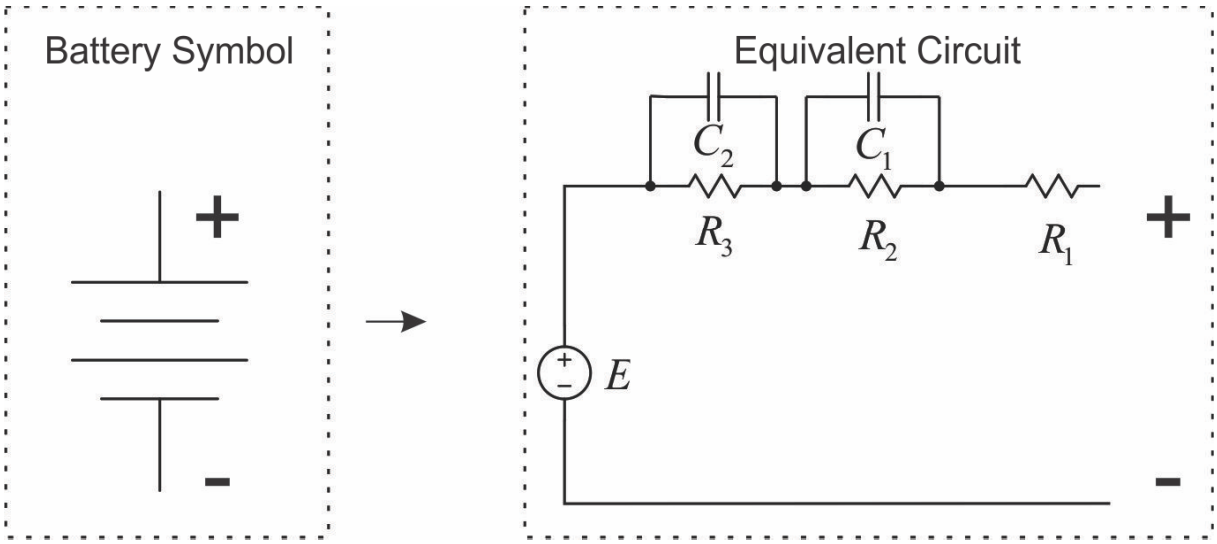
Source: (WANG, 2009)

The State of Charge (SoC) indicates the percentage of charge remaining on the battery. On the other hand, the Depth of Discharge (DoD), which is the complement of

SoC, indicates the percentage already consumed. The State of Health (SoH) indicates the energy storage capacity of a battery compared with a new one. As more charging cycles the battery has, as lower will be its SoH.

Figure 2.2 shows the equivalent electric circuit of a battery. It is composed of a voltage source, which depends on SoC, and an association of resistors and capacitors. For low frequencies, its impedance is dominated by the resistors. For frequencies in the Hz to kHz range, the circuit starts to present the capacitors' dynamic influence. For higher frequencies, beyond capacitors dynamic, the skin effect is noted, which increases the resistance of the circuit.

Figure 2.2 – Equivalent electrical circuit of a battery



Source: Own elaborated

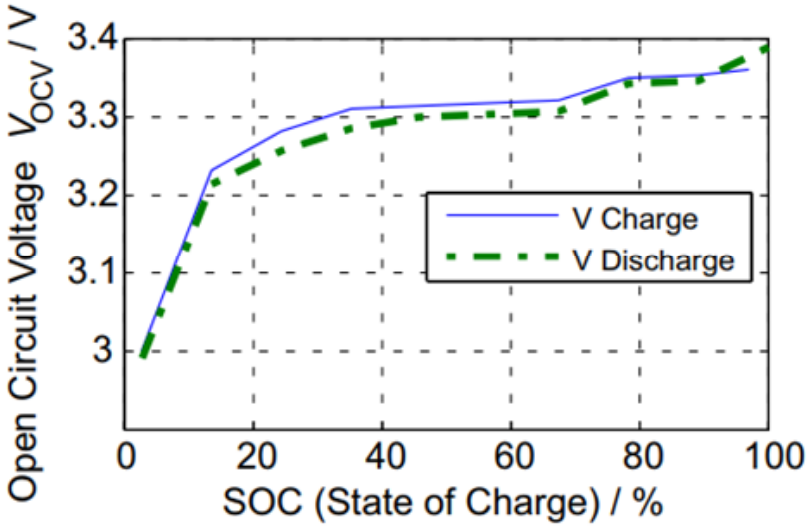
In addition to the advantages of LIB among other energy accumulators, it requires accurate monitoring of voltage, current, and temperature. These systems are called the Battery Management System (BMS). It will protect the battery from critical levels of operation mentioned before (KIM; KWON; HYUN, 2012).

To estimate the SoC, it can be used as a method that verifies the amount of current inserted and extracted from the battery, given a known initial state, as used by the authors (HAN, 2016) and (TOPAN et al., 2016). In that way, this method requires recursive equations to estimate SoC. Due to the uncertainties of the results, its implementation presents high complexity.

Another method used by (CHEN; RINCON-MORA, et al., 2006) estimates the SoC through voltage intervals presented on the battery terminals, as seen in Figure 2.3. Besides the existence of different methods (KIM; KWON; HYUN, 2012; HAN, 2016; TOPAN et al., 2016; THOMAS; STIENEKER; DE DONCKER, 2013), its charging is divided into two stages. The first step charges the battery with a constant current until

it reaches a given voltage. Once reached the voltage, the second phase starts to drop the current without changing the terminal voltage.

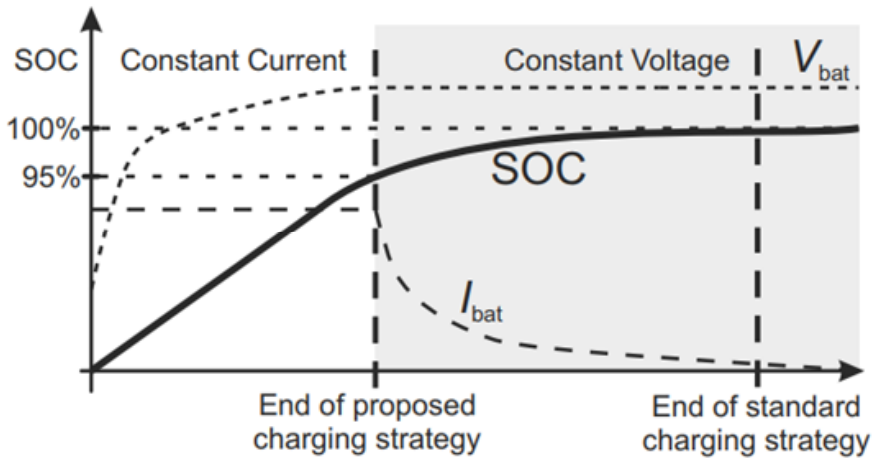
Figure 2.3 – State of Charge (SoC) vs Voltage in charge and discharge



Source: (THOMAS; STIENEKER; DE DONCKER, 2013)

This charging method avoids the extrapolation of current and voltage allowed in the LIB. This can be seen in Figure 2.4, presented by (THOMAS; STIENEKER; DE DONCKER, 2013).

Figure 2.4 – Constant Voltage - Constant Current Charging Strategy

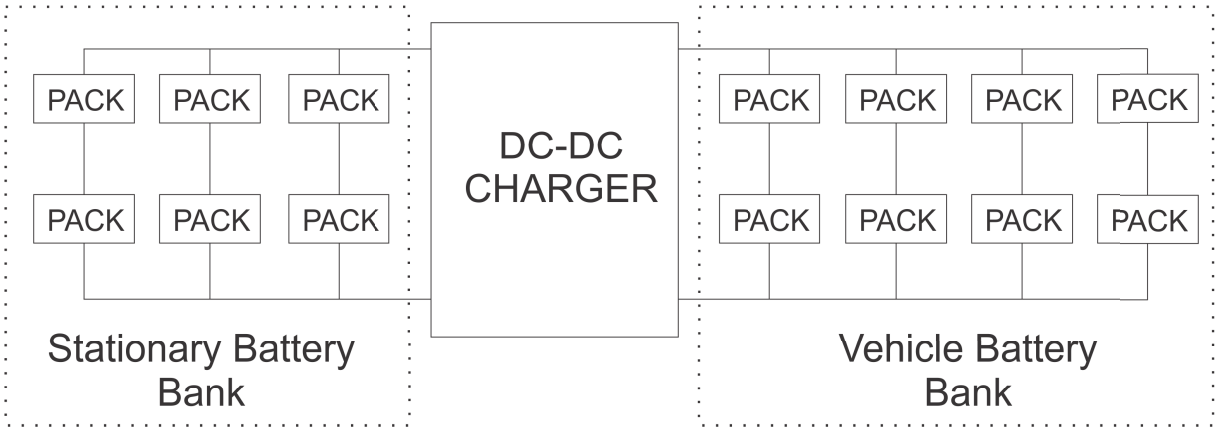


Source: (THOMAS; STIENEKER; DE DONCKER, 2013)

2.2 BATTERY BANK MODEL

The architecture consists of two battery banks: one stationary and the other located in the vehicle exemplified in Figure 2.5. The energy flow takes place from the stationary bank to the vehicle, controlled by a DC-DC converter. The State of Charge (SoC) of each battery bank may change considerably its terminal voltage.

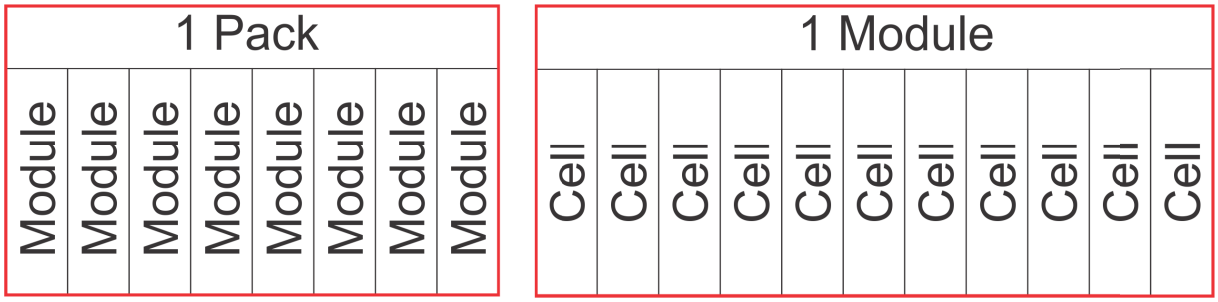
Figure 2.5 – Implemented Architecture



Source: Own elaborated

The implemented architecture is formed by the connection two battery banks, one inside the E-bus and the other in the charging station. The stationary bank has three strings parallel-connected, while the vehicle's battery bank has four strings, as shown in Figure 2.5. Each pack is composed of the connection of eight battery modules in series. And each battery module is the arrangement of 11 battery cells, also series-connected. This model is presented in Figure 2.6.

Figure 2.6 – Battery Pack Internal Structure



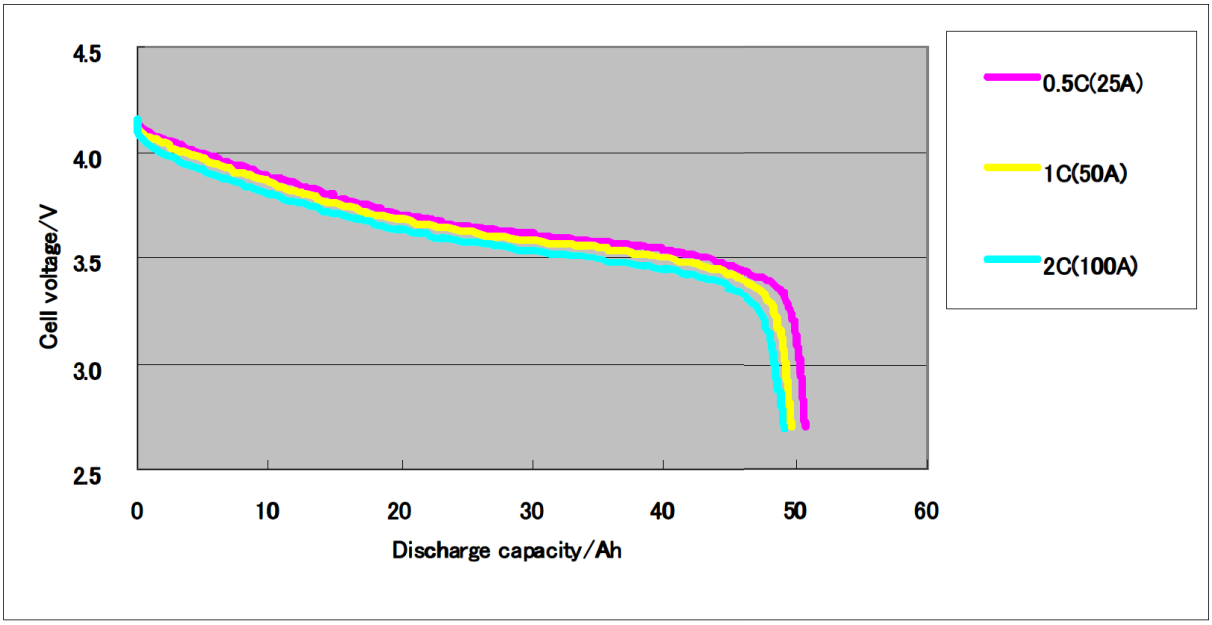
Source: Own elaborated

According to the manufacturer's datasheet, the charge and discharge curves show the battery's cell operating characteristics, along with its operating limits. Among them, the following information stands out:

- Voltage limits: 2.7 to 4.15 V
- Maximum Charging/Discharging:
  - Continuous: 100 A at 25 °C
  - Transitory: 300 A at 25 °C during 10 s
- Capacity: 185 Wh or 50 Ah (at 25 °C)

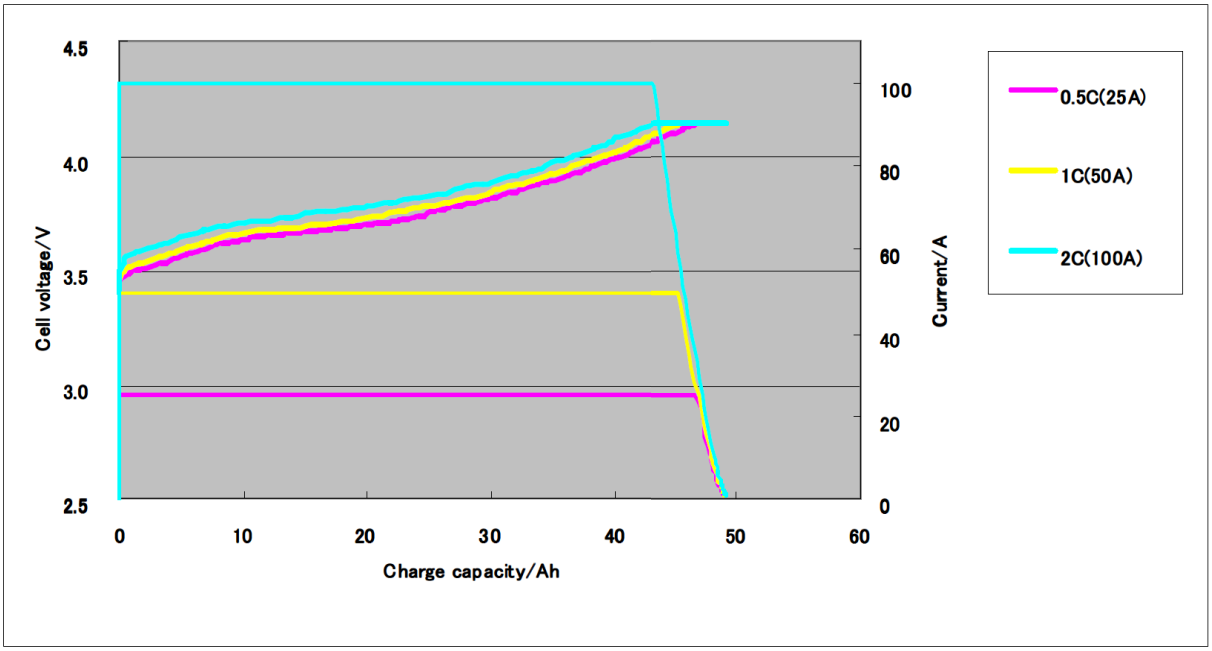
Figure 2.7 shows the cell voltage according to the discharge current. Also is presented the variation of discharge capacity. On the other hand, Figure 2.8 presents the battery cell voltage, given charging current. It is important to see that, when reached a certain voltage, the current used to charge is reduced to avoid battery cell overvoltage, which can damage it.

Figure 2.7 – Cell voltage vs discharge capacity



Source: Manufacturer datasheet

Figure 2.8 – Cell voltage vs charge capacity

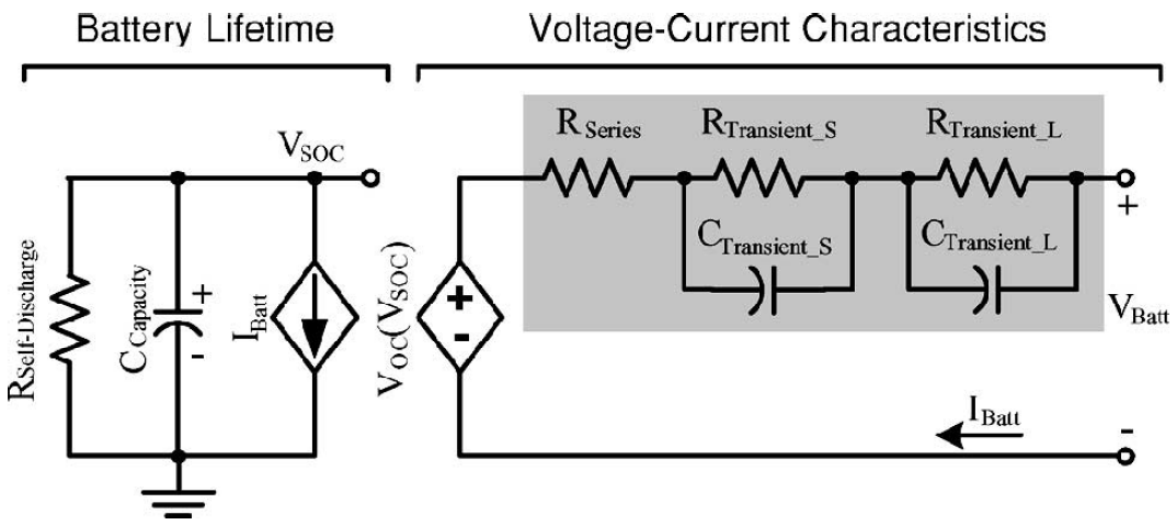


Source: Manufacturer datasheet

2.3 EQUIVALENT ELECTRICAL CIRCUIT

A battery model presented by (CHEN; RINCON-MORA, et al., 2006) shows the equivalent circuit with a voltage-controlled source. Also, the resistors and capacitors may vary according to its SoC. This is exemplified in Figure 2.9.

Figure 2.9 – Equivalent electrical circuit of a LIB



Source: (CHEN; RINCON-MORA, et al., 2006)

In (CHEN; RINCON-MORA, et al., 2006), it is extracted numerical values for an 850 mAh battery. Their obtained values are shown:

$$\begin{aligned} V_{OC}\left(SOC\right) = -1.031 \cdot \left(e^{-35 \cdot SOC}\right) + 3.685 + \\ +0.2156 \cdot SOC - 0.1178 \cdot \left(SOC\right)^2 + 0.3201 \cdot \left(SOC\right)^3 \end{aligned} \tag{2.1}$$

$$R_{Series}\left(SOC\right) = 0.1562 \cdot e^{-24.37 \cdot SOC} + 0.07446\ [\Omega] \tag{2.2}$$

$$R_{Transient_S}\left(SOC\right) = 0.3208 \cdot e^{-29.14 \cdot SOC} + 0.04669\ [\Omega] \tag{2.3}$$

$$C_{Transient_S}\left(SOC\right) = -752.9 \cdot e^{-13.51 \cdot SOC} + 703.6\ [F] \tag{2.4}$$

$$R_{Transient_L}\left(SOC\right) = 6.603 \cdot e^{-155.2 \cdot SOC} + 0.04984\ [\Omega] \tag{2.5}$$

$$C_{Transient_L}\left(SOC\right) = -6056 \cdot e^{-27.12 \cdot SOC} + 4475\ [F] \tag{2.6}$$

$$C_{Capacity} = 3600 \cdot 0.850 = 3060\ [F] \tag{2.7}$$

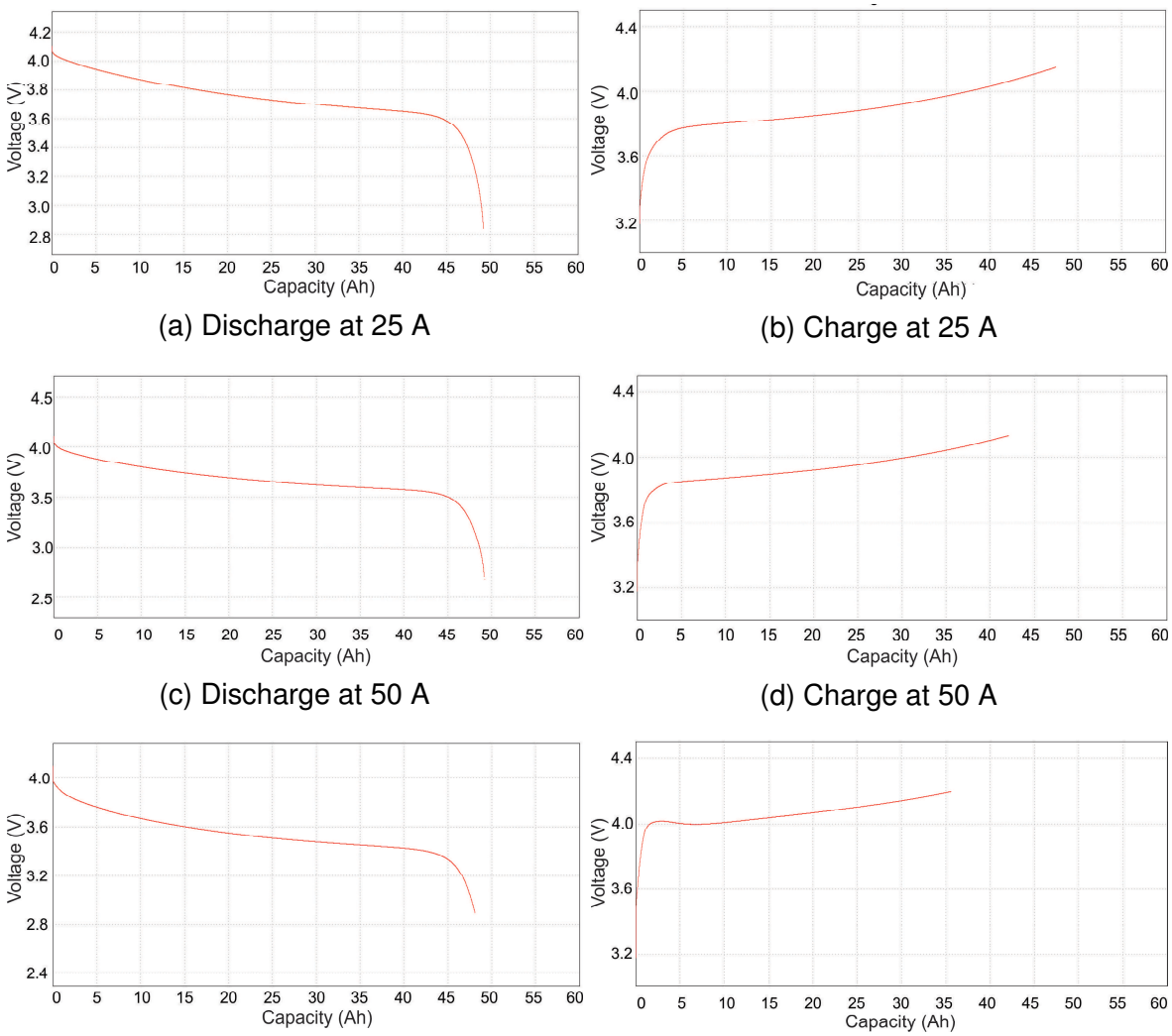
The self-discharge resistance was ignored. Following the equations of (CHEN; RINCON-MORA, et al., 2006), the values were adapted for the cell used in the proposed architecture, whose capacity is 50 Ah. Then, the battery studied by the author was used as the basis. To adapt it to the model of this thesis, an adjustment factor was proposed in order to simulate the batteries of (CHEN; RINCON-MORA, et al., 2006) connected in parallel. This factor can be easily calculated as shown in equation (2.8).

$$F_{adjust} = \frac{50}{0.850} = 58.82 \tag{2.8}$$

This F_{adjust} factor will be used to estimate the equivalent capacitors and resistors in parallel.

The V_{OC} voltage does not need to be adjusted, once the parallel value has no change. Using the adjusting factor through software aided, it was found the charging and discharging curves for the used battery bank, shown in Figure 2.10.

Figure 2.10 – Open Circuit Voltages according SOC - Computational Simulation



(a) Discharge at 25 A

(b) Charge at 25 A

(c) Discharge at 50 A

(d) Charge at 50 A

(e) Discharge at 100 A

(f) Charge at 100 A

Source: Own elaborated

The curves found, based on (CHEN; RINCON-MORA, et al., 2006) article and shown in Figure 2.10, presents the charging and discharging characteristics of the battery. Comparing the values found through simulation with the datasheet (Figures 2.7 and 2.8), the model approximates the real values, diverging only in Figure 2.10f.

Then, it is used this computational model to simulate the structure. The voltage variation expected by simulation will change according to the below equations:

$$V_{bat_min} = 2.7(V)x8(cells)x11(mod.)x2(packs) \tag{2.9}$$

$$V_{bat_min} = 475.2V \tag{2.10}$$

$$V_{bat_max} = 4.15(V)x8(cells)x11(mod.)x2(packs) \tag{2.11}$$

$$V_{bat_max} = 730.4V \tag{2.12}$$

Besides its minimum value found is 475,2 Volts, the manufacturer does not recommend using the batteries below 526 Volts. Therefore, the value used to project the converter follows the specification given by the manufacturer.

Also, it must be calculated the maximum allowed currents for charging and discharging, given the used architecture. As a single cell has a capacity of 100 A of discharge, it is obtained the following values.

The maximum discharging current of stationary bank:

$$I_{max_{dschg}} = 100(A)x3(packs) = 300A \tag{2.13}$$

The maximum charging current of the automotive bank:

$$I_{chg} = 100(A)x4(packs) = 400A \tag{2.14}$$

From these values, it can be obtained the maximum power extracted from the stationary bank; and the maximum power delivered to automotive batteries.

$$P_{in_max} = 730.4x300 = 219.12kW \tag{2.15}$$

$$P_{out_max} = 730.4x400 = 292.16kW \tag{2.16}$$

2.4 PARTIAL CONCLUSIONS

It can be easily verified the reason for the popularization of lithium batteries. With its high energy density, it became a water divisor for the communication system and electrical mobility.

In this way, it is possible to notice that not only the lithium batteries show excellent characteristics as an energy accumulator, but also has a simple electrical model to be implemented, which allows the application of control techniques and it avoids undesired operating conditions. Therefore, knowing the storage system becomes crucial for choosing the topology of the converter and stipulating its operating parameters.

Also, a very precise regulation of voltage and current is needed, once that getting out of its safe operating region can permanently damage the batteries.

3 LITERATURE REVIEW OF CONVERTERS FOR BATTERY CHARGING

Battery chargers can be characterized by the charging method which is used and also by how the charger connects to the grid.

The battery charging method can be divided into two groups: slow charge, which can take between six to eight hours to a complete vehicle charge; and fast charge, defined as other than slow charge (BOTSFORD; SZCZEPANEK, 2009). Table 3.1 presents an example of power rated converters given a standard vehicle model.

Table 3.1 – Power Levels for DC Charging

Type of Charge	**Charger Power Level (kW)**		
	Heavy Duty	**SUV/Sedan**	**Small Sedan**
Fast Charge, 10 minutes, 100% SoC	500	250	125
Rapid Charge, 15 minutes, 60% SoC	250	125	60
Quick Charge, 60 minutes, 70% SoC	75	35	20
Plug-In Hybrid, 30 Minutes	40	20	10

Source: (BOTSFORD; SZCZEPANEK, 2009)

This division presented in Table 3.1 relates the battery capacity of the vehicle and the power rated of the charger. This means that a power converter can not be classified in slow or fast charger just by its power, but with the interaction with the battery to be charged.

As mentioned, the charger can be characterized by how it is connected to the power grid. The Society of Automotive Engineers (SAE) defines the SAE J-1772, which is the standard for connectors on a plug-in vehicle. The connectors are divided into three levels:

- Level 1 – 120V AC;
- Level 2 – 120V and 240V AC; and
- Level 3 – DC up to 550A, 600V.

Level 1 is typically categorized for residential use. Generally, they are unidirectional converters that use the residential electrical grid to carry out charging at low power levels.

At level 2 the processed power is higher than level 1 and the use can be residential and commercial (YILMAZ; KREIN, 2013). For levels 1 and 2 the chargers are generally of the on-board type.

Level 3 is used for fast battery charging. Therefore, the power levels are higher compared to levels 1 and 2, which increases the equipment size. Thus, these chargers are of the off-board type, in other words, they are not located in the vehicle. Level 3

chargers are usually connected to a three-phase grid with active rectifiers for power factor correction and harmonic suppression (KUPERMAN et al., 2010).

One of the advantages of using off-board loading is the reduction in weight and volume of equipment present in the vehicle. In contrast, it is often necessary to make changes to the connections to the grid, such as charging cables and protective equipment.

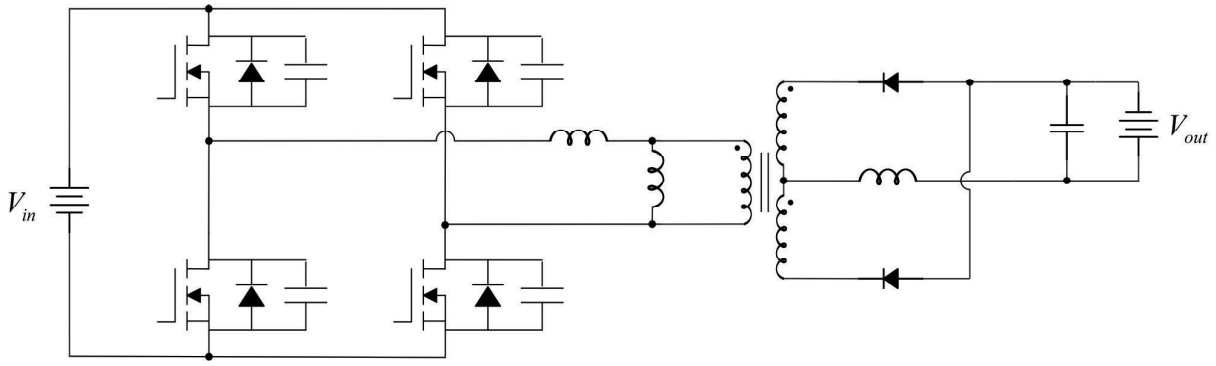
To avoid the use of a specific connection to the grid, that allows to drain large amounts of energy in a short time interval, it is possible to use an external battery station.

3.1 BATTERY CHARGERS TOPOLOGIES

There are several studies on battery chargers focused on several purposes, such as the speed at which they charge, efficiency, galvanic isolation, weight reduction, reduction of the number of semiconductors, and reduction of the volume of magnets.

Thus, several converters are applicable to the proposed architecture, each with its particularity of optimization parameters. One of them is the phase-shifted full-bridge converter, presented by (CETIN; ASTEPE, 2016) and shown in Figure 3.1. This converter allows the galvanic insulation and also the operation in soft commutation without adding elements to the structure.

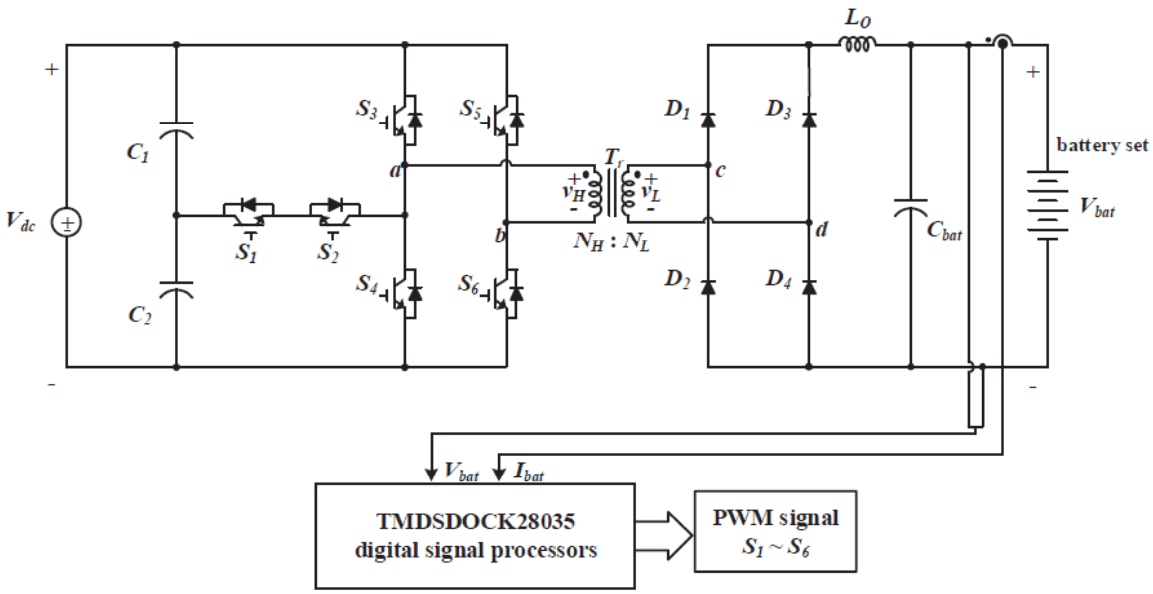
Figure 3.1 – Phase-Shifted Full-Bridge



Source: Own elaborated

Another interesting converter is the converter stated by (JOU et al., 2018), an asymmetrical T-type DC-DC converter that has galvanic insulation, and that reduces the voltage stress on the semiconductors. It is also a four-level DC-DC converter that allows the EMI filter reduction. Its topology is presented in Figure 3.2.

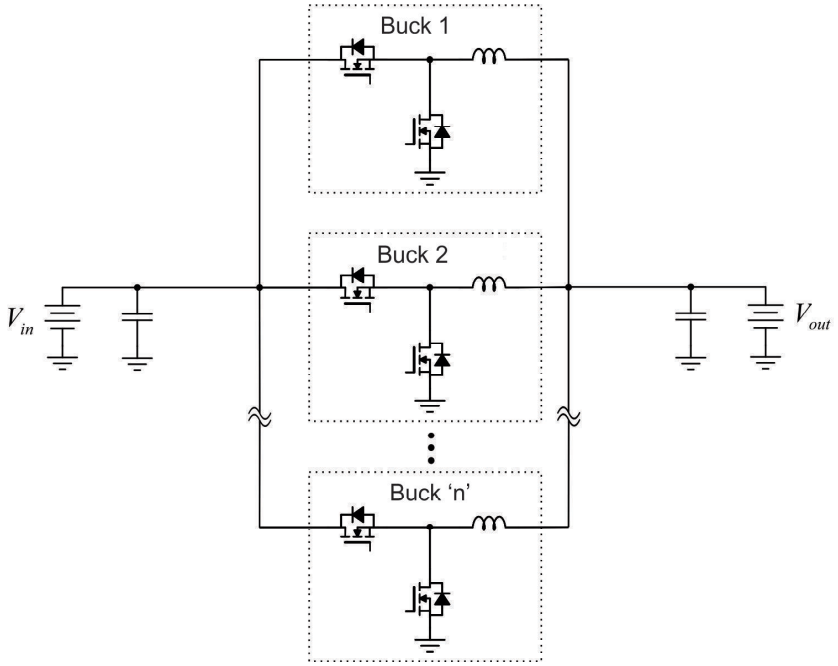
Figure 3.2 – Asymmetrical T-type Isolated Four-Level DC-DC Battery Charger



Source: (JOU et al., 2018)

Another interesting proposal is presented by (GARCÍA et al., 2006) which uses a bidirectional interleaved Buck converter shown in Figure 3.3. The author presents the efficiency analysis given the number of channels used. The conclusion is that this technique is always appropriated to reach better dynamic response, filter reduction, and better thermal management (GARCÍA et al., 2006).

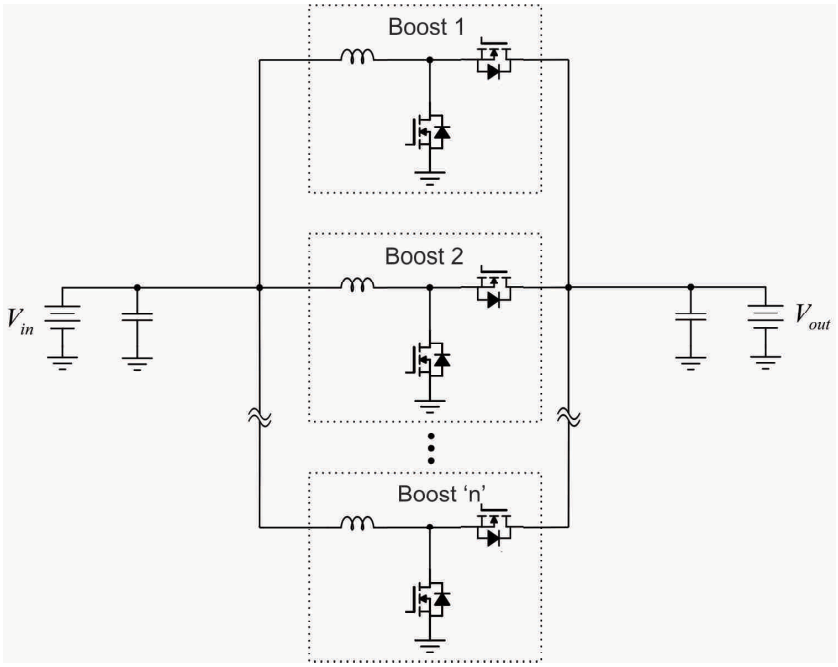
Figure 3.3 – Interleaved Buck Converter



Source: Own Elaborated

The topology presented in Figure 3.4, by (NI; PATTERSON; HUDGINS, 2010; WANG, 2009) is a bidirectional interleaved Boost. It is characterized as a step-up converter and it has the same advantages of the Buck by its interleaved connection.

Figure 3.4 – Interleaved Boost converter



Source: Own elaborated

The converters Buck and Boost are classical topologies used to step down and step up the output voltages. They can be represented of one switch and one diode for the semiconductors. Figures 3.3 and 3.4, they are represented using two switches each allowing the operation for bidirectional power flow. Thus, the Buck converter is also a Boost converter if operated in the reverse power flow. Similarly Boost is a Buck converter when operating with negative current in the input.

The advantage of using interleaved converters is the shared electric current in the input and output by each level, allowing the use of the same filters. Thus, it is mandatory to equalize the power in each channel, in face the oscillations in the external connections. This is not a problem if the converter operates in Discontinuous Conduction Mode (DCM), wherein external variations does not vary significantly at the current peak. Still, the digital electronic progress makes the operation of those converters easy and viable (GARCÍA et al., 2006), even for Continuous Conduction Mode (CCM). Reinforced by (MUSAVI et al., 2011; NI; PATTERSON; HUDGINS, 2010; WANG, 2009; CREWS, 2013; O'LOUGHLIN, 2006), the interleaving techniques for processing energy are advantageous.

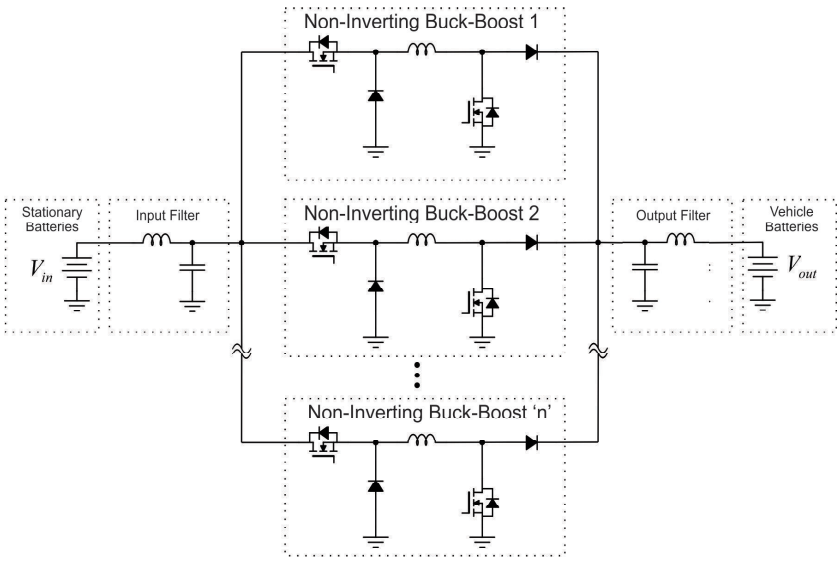
There is a need to use filters at the input and output of the converter so that the high frequency caused by the switching of the semiconductors does not affect the battery life. In parallel, it requires the inclusion of an EMI filter to respect the standards. One way to decrease the filter would be to increase the switching frequency (NI; PATTERSON; HUDGINS, 2010). However, with the interleaving technique, it is possible to reduce the filter while maintaining the frequency of operation. According to (NI; PATTERSON; HUDGINS, 2010; WANG, 2009) the technique also allows the effective current on the capacitors to be reduced, making the converter more robust.

Among several battery charger topologies, the main requirements for the converter inside the proposed architecture are: a non-inverting output and to operate as a step-up and step-down charger.

Based on the design requirements, it is necessary to have a converter that presents elevating and lowering characteristics to fulfill the desired function, realizing the variations in voltages in the system according to the SoC of the batteries. Thus, the converter to be analyzed and dimensioned is the Non-Inverting Buck-Boost Converter presented in Figure 3.5, which allows the step-up and step-down voltage conversion.

In this thesis is presented a design of a higher power rated non-inverting Buck-Boost converter, with a droop control method, proving its feasibility. This converter has already its advantages tested and verified by (NICOLLI, 2019).

Figure 3.5 – Interleaved Non-Inverting Buck-Boost converter



Source: Own elaborated

3.2 PARTIAL CONCLUSIONS

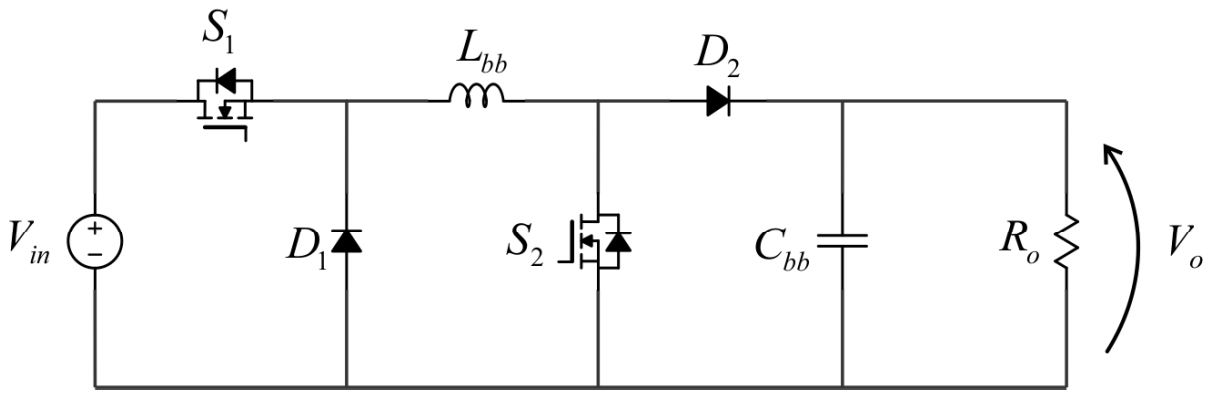
Altogether, a battery charger is characterized by its transfer power rate along with the type of its charge. Different topologies can meet the needs of the project. The Non-Inverter Buck-Boost (NIBB) converter stood out due to its simplicity, its reduced number of semiconductors, and the absence of transformers.

Depending on the type of modulation used, the NIBB converter can operate as a cascade Buck and Boost converters, or as a conventional Buck-Boost. In the following chapters, the study of this converter is presented for both operation modes, its waveforms, and its mathematical modeling, justifying the choice made.

4 STUDY OF NON-INVERTING BUCK-BOOST CONVERTER IN CONTINUOUS CONDUCTION MODE

The Non-Inverting Buck-Boost topology is formed by four semiconductors: two diodes and two switches. The Figure 4.1 reveals its topology with a voltage source and a load resistor.

Figure 4.1 – Non-inverting Buck-Boost Topology



Source: Own elaborated

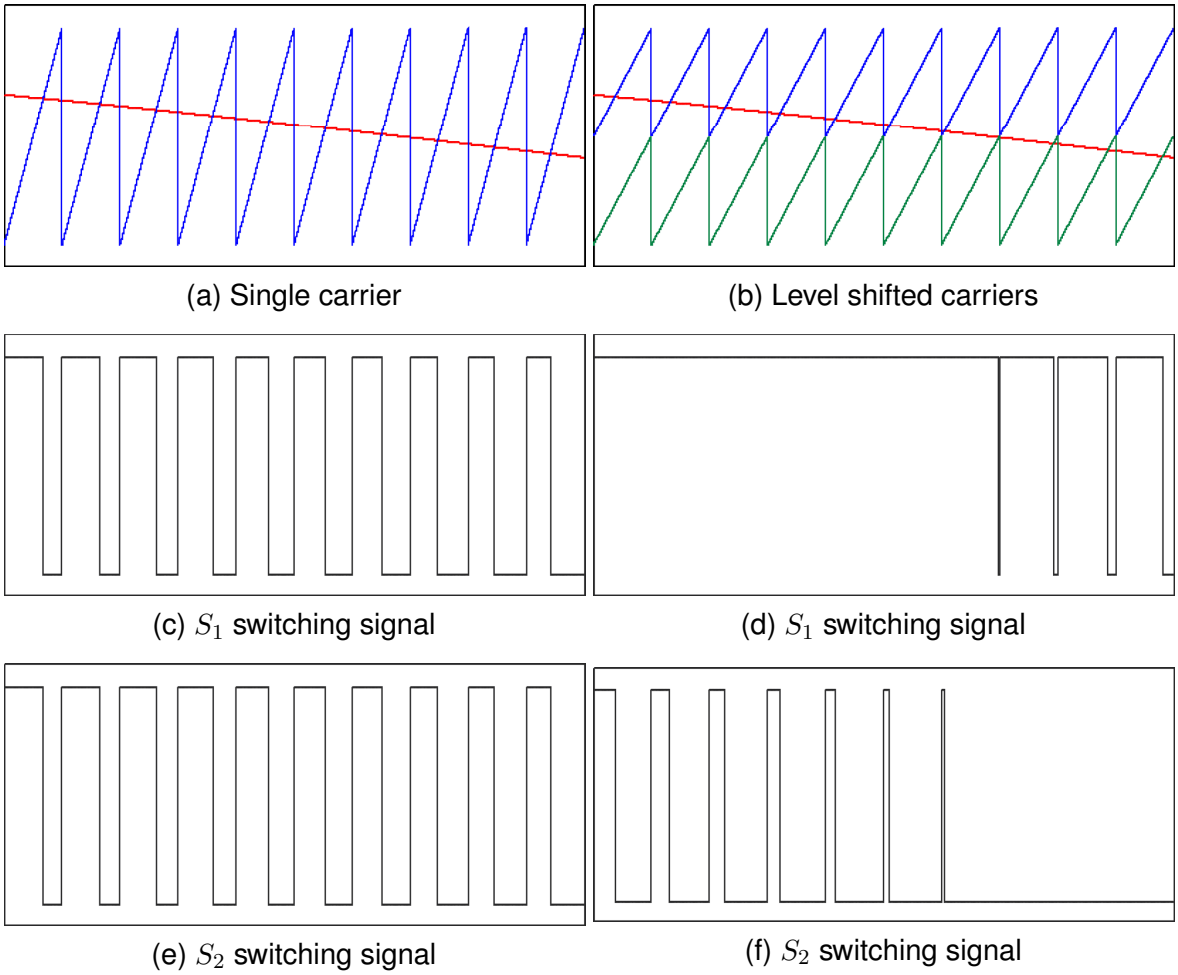
4.1 MODULATION

There are two main techniques to modulate the non-inverting Buck-Boost, as shown in Figure 4.2.

The first is to set the same gate signal for both switches. To perform that, it is necessary only one carrier signal, as appears in Figure 4.2a.

The second technique is to set two carriers level-shifted, allowing the operation of only one switch according to the modulation signal, seen in Figure 4.2b. The Figures 4.2d and 4.2f present gate signals of switches S_1 and S_2, respectively.

Figure 4.2 – Modulation signal, Carrier, and PWM Pulse



(a) Single carrier (b) Level shifted carriers

(c) S_1 switching signal (d) S_1 switching signal

(e) S_2 switching signal (f) S_2 switching signal

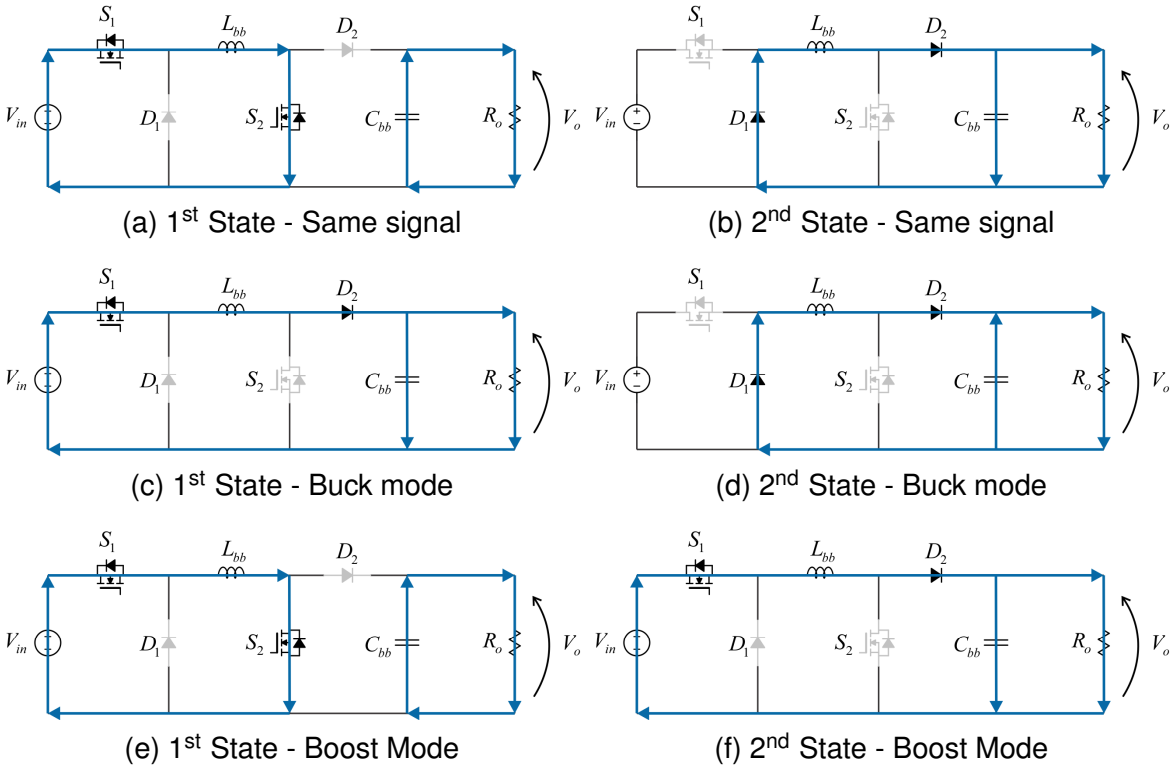
Source: Own elaborated

4.2 TOPOLOGICAL STATES

Each of the two modulation techniques will lead to different topological states. When setting the same switching signal, the first interval the diodes are blocked and the input voltage is imposed on the inductor, shown in Figure 4.3a. In the next stage, the switches are blocked and the diodes start conducting, seen in Figure 4.3b.

However, when used the level-shifted carriers, the converter will operate as a Buck converter if the modulation signal is on the lower carrier. If the modulation signal is on the upper carrier, it will operate as a Boost converter. This is presented in Figures 4.3c, 4.3d, 4.3e, and 4.3f.

Figure 4.3 – Topological States of a Non-inverting Buck-Boost



(a) 1st State - Same signal

(b) 2nd State - Same signal

(c) 1st State - Buck mode

(d) 2nd State - Buck mode

(e) 1st State - Boost Mode

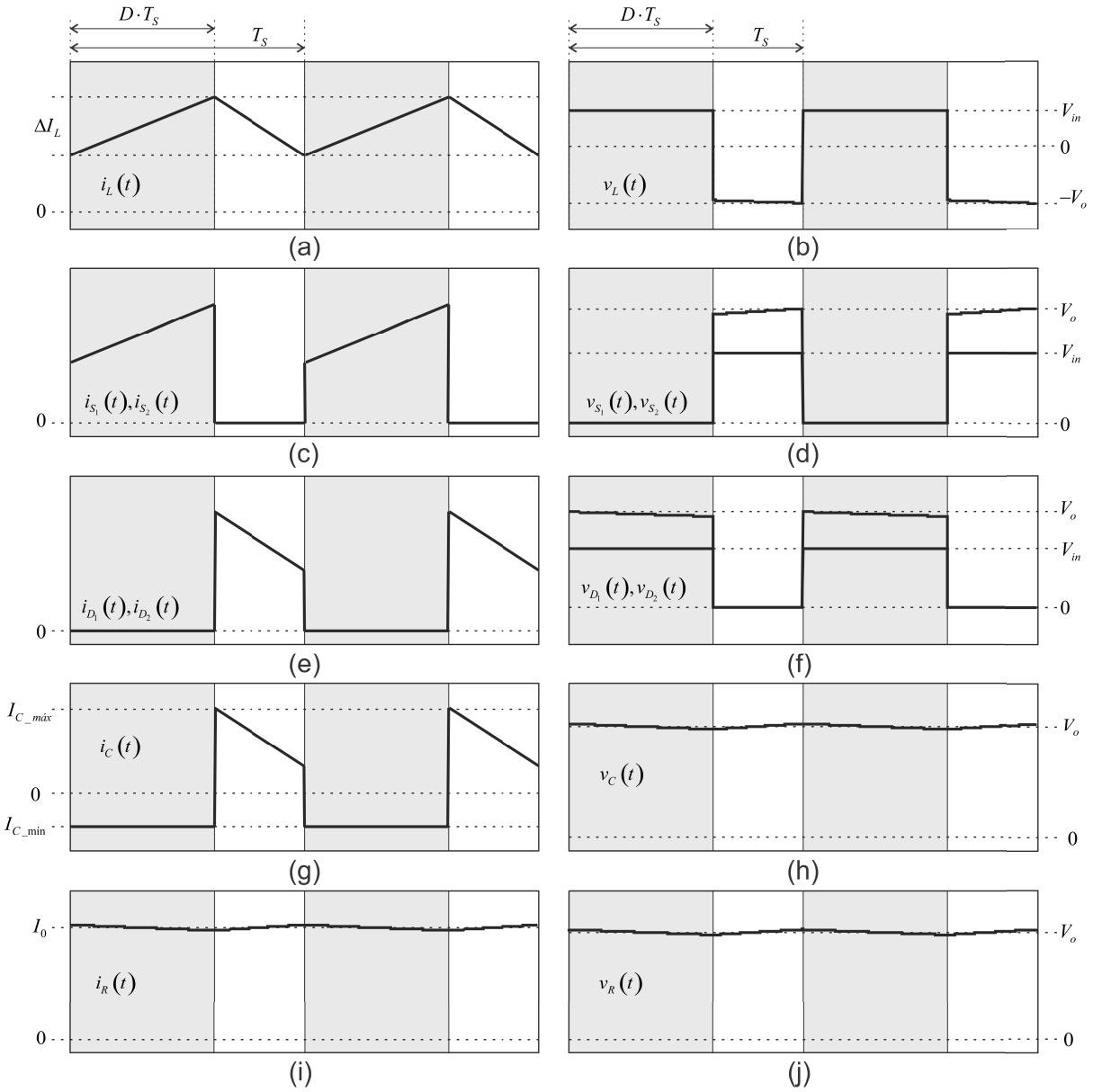
(f) 2nd State - Boost Mode

Source: Own elaborated

4.3 WAVEFORMS

Once presented the different topological states as a consequence of the modulation technique chosen, from now on all the content is considered the same gate signal set on the switches. In the next chapters is presented a study of Buck and Boost operation, separately.

Figure 4.4 – Converter Waveforms



Source: Own elaborated

The waveforms of the Buck-Boost converter are shown in Figure 4.4:

- current 4.4a and voltage 4.4b on the inductor;
- current 4.4c and voltage 4.4d on the switch;
- current 4.4e and voltage 4.4f on the diode;
- current 4.4g and voltage 4.4h on the capacitor;
- current 4.4i and voltage 4.4j at load resistor.

4.4 ALGEBRAIC ANALYSIS

The algebraic analysis were done for the operation in continuous condition mode. Assuming that the average voltage over the inductor is zero in a switching period during steady-state operation, the static gain can be found from:

$$\langle v_L \rangle_{T_S} = D \cdot V_{in} + (1 - D) \cdot V_o \tag{4.1}$$

Solving equation (4.1):

$$\frac{V_o}{V_{in}} = \frac{D}{1 - D} \tag{4.2}$$

Rearranging equation, the duty cycle of a load resistance is given by:

$$D = \frac{V_o}{V_{in} + V_o} \tag{4.3}$$

Assuming that there are no losses on the circuit:

$$V_o \cdot I_o = V_{in} \cdot I_{in} \tag{4.4}$$

Replacing (4.2) in (4.4), it is found the relation between currents:

$$\frac{I_{in}}{I_o} = \frac{D}{1 - D} \tag{4.5}$$

4.4.1 Inductor

In the interval DT_S to T_S, the ripple voltage over the inductor can be described as:

$$v_{L_{bb}} = L_{bb} \frac{di_{L_{bb}}}{dt} \tag{4.6}$$

$$V_{in} = L_{bb} \frac{\Delta i_{L_{bb}}}{D \cdot T_S} \tag{4.7}$$

Hence:

$$\Delta i_{L_{bb}} = \frac{V_{in} \cdot D}{L_{bb} \cdot f_S} \tag{4.8}$$

Rearranging the equation terms, the inductor can be sized as:

$$L_{bb} = \frac{V_{in} \cdot D}{\Delta i_{L_{bb}} \cdot f_S} \tag{4.9}$$

The average current on the inductor can be calculated from Figure 4.4, wherein:

$$I_{in} = I_{L_{bb}} \cdot D \tag{4.10}$$

$$I_o = I_{L_{bb}} \cdot (1 - D) \tag{4.11}$$

Then:

$$I_{in} + I_o = (I_{L_{bb}} \cdot D) + [I_{L_{bb}} \cdot (1 - D)] \tag{4.12}$$

Hence:

$$I_{L_{bb}} = I_{in} + I_o \tag{4.13}$$

4.4.2 Capacitor

The ripple voltage over the non-inverting Buck-Boost can be defined as:

$$i_{C_{bb}} = C_{bb} \frac{dv_{C_{bb}}}{dt} \tag{4.14}$$

On interval from 0 tp DT_S, the diode is blocked. Consequently, the capacitor must provide the average current for the load. Then:

$$I_o = C_{bb} \frac{\Delta v_{C_{bb}}}{D \cdot T_S} \tag{4.15}$$

So the ripple voltage can be described as:

$$\Delta v_{C_{bb}} = \frac{I_o \cdot D}{C_{bb} \cdot f_S} \tag{4.16}$$

Rearranging the equation (4.16), the capacitor can be sized as:

$$C_{bb} = \frac{I_o \cdot D}{\Delta v_{C_{bb}} \cdot f_S} \tag{4.17}$$

4.4.3 Switches

As the switches are being commanded by the same signal, when closed they are inside the same loop in the first topological state. Consequently, the current in both will be the same, as shown in Figure 4.4c. Then, the average current can be calculated as:

$$I_S = \frac{1}{T_S} \int_0^{T_S} i_S(t) \cdot dt \tag{4.18}$$

During the closed interval, the current on the switches is the same current on the inductor. In the remaining time, the switches are blocked and the current goes to zero. Thus:

$$I_S = \frac{1}{T_S} \int_0^{DT_S} i_{L_{bb}}(t) \cdot dt \tag{4.19}$$

The current on the inductor can be defined as:

$$i_{L_{bb}}(t) = \begin{cases} I_{L_{bb}} - \frac{\Delta i_{L_{bb}}}{2} + \frac{V_{in} \cdot t}{L_{bb}} & if \quad t < DT_S \\ I_{L_{bb}} - \frac{\Delta i_{L_{bb}}}{2} - \frac{V_o \cdot (t - DT_S)}{L_{bb}} & if \quad t > DT_S \end{cases} \tag{4.20}$$

The average current on the inductor is the sum of average input and output current.

$$I_L = I_{in} + I_o \tag{4.21}$$

Using the relation of equation (4.5) in (4.21):

$$I_{L_{bb}} = \frac{I_{in}}{D} \tag{4.22}$$

So, in the interval from 0 to DT_S, according with equations (4.22) and (4.8), the current on the inductor is:

$$i_{L_{bb}}(t) = \frac{I_{in}}{D} - \frac{V_{in} \cdot D}{2 \cdot L_{bb} \cdot f_S} + \frac{V_{in} \cdot t}{L_{bb}} \tag{4.23}$$

Thus, the average current is obtained from:

$$I_S = \frac{1}{T_S} \int_0^{DT_S} \left(\frac{I_{in}}{D} - \frac{V_{in} \cdot D}{2 \cdot L_{bb} \cdot f_S} + \frac{V_{in} \cdot t}{L_{bb}} \right) \cdot dt \tag{4.24}$$

Solving equation (4.23):

$$I_S = I_{in} \tag{4.25}$$

The RMS current on the switch can be calculated by:

$$I_{S_ef} = \sqrt{\int_0^{T_S} \frac{1}{T_S} [i_S(t)]^2 \cdot dt} \tag{4.26}$$

As the switch current is equal to inductor current in the first interval:

$$I_{S_ef} = \sqrt{\int_0^{DT_S} \frac{1}{T_S} [i_{L_{bb}}(t)]^2 \cdot dt} \tag{4.27}$$

$$I_{S_ef} = \sqrt{\int_0^{DT_S} \frac{1}{T_S}\left[\frac{I_{in}}{D} - \frac{V_{in}\cdot D}{2\cdot L_{bb}\cdot f_S} + \frac{V_{in}\cdot t}{L_{bb}}\right]^2 \cdot dt} \tag{4.28}$$

Solving equation (4.28):

$$I_{S_ef} = \sqrt{\frac{I_{in}^2}{D} + \frac{D^3\cdot V_{in}^2\cdot T_S}{12\cdot {L_{bb}}^2}} \tag{4.29}$$

Besides the currents be the same on switches, the reverse voltage in each switch is different: when they are blocked in the interval from DT_S to T_S, V_in is applied to S_1, while V_o is applied to S_2.

$$V_{S_{1_}\max} = V_{in} \tag{4.30}$$

$$V_{S_{2_}\max} = V_o \tag{4.31}$$

4.4.4 Diodes

The average current in diodes can be calculated from:

$$I_D = \frac{1}{T_S}\int_0^{T_S} i_D\,(t)\cdot dt \tag{4.32}$$

The diode current in the DT_S to T_S is equal to the inductor current.

$$I_D = \frac{1}{T_S}\int_{DT_S}^{T_S} i_{L_{bb}}\,(t)\cdot dt \tag{4.33}$$

The current on the inductor from D_TS to D_TS is equal to:

$$i_{L_{bb}}\,(t) = \frac{I_{in}}{D} + \frac{V_{in}\cdot D}{2\cdot L_{bb}\cdot f_S} - \frac{V_{in}\cdot D\cdot (t-DT_S)}{(1-D)\cdot L_{bb}} \tag{4.34}$$

Replacing (4.34) in (4.33):

$$I_D = \frac{1}{T_S}\int_{DT_S}^{T_S}\left(\frac{I_{in}}{D} + \frac{V_{in}\cdot D}{2\cdot L_{bb}\cdot f_S} - \frac{V_{in}\cdot D\cdot (t-DT_S)}{(1-D)\cdot L_{bb}}\right)\cdot dt \tag{4.35}$$

Solving equation (4.35):

$$I_D = I_o \tag{4.36}$$

The RMS current on the diodes can be defined from:

$$I_{D_ef} = \sqrt{\int_0^{T_S} \frac{1}{T_S}[i_D(t)]^2 \cdot dt} \tag{4.37}$$

Then:

$$I_{D_ef} = \sqrt{\int_{DT_S}^{T_S} \frac{1}{T_S}[i_{L_{bb}}(t)]^2 \cdot dt} \tag{4.38}$$

$$I_{D_ef} = \sqrt{\int_{DT_S}^{T_S} \frac{1}{T_S}\left[\frac{I_{in}}{D} + \frac{V_{in}\cdot D}{2\cdot L_{bb}\cdot f_S} - \frac{V_{in}\cdot D\cdot(t-DT_S)}{(1-D)\cdot L_{bb}}\right]^2 \cdot dt} \tag{4.39}$$

Solving equation (4.39), it is found:

$$I_{D_ef} = \sqrt{\frac{(1-D)\cdot(D^4\cdot V_{in}^2\cdot T_S^2 + 12\cdot I_{in}^2\cdot L_{bb}^2)}{12\cdot D^2\cdot L_{bb}^2}} \tag{4.40}$$

Similarly to the Buck-Boost switches, the diodes will have the same current, and the reverse voltage applied is different among them. In a blocked state, the reverse voltage on the diode D_1 is the input voltage, while on the diode D_2 is the output voltage.

$$V_{D_{1_}\max} = V_{in} \tag{4.41}$$

$$V_{D_{2_}\max} = V_o \tag{4.42}$$

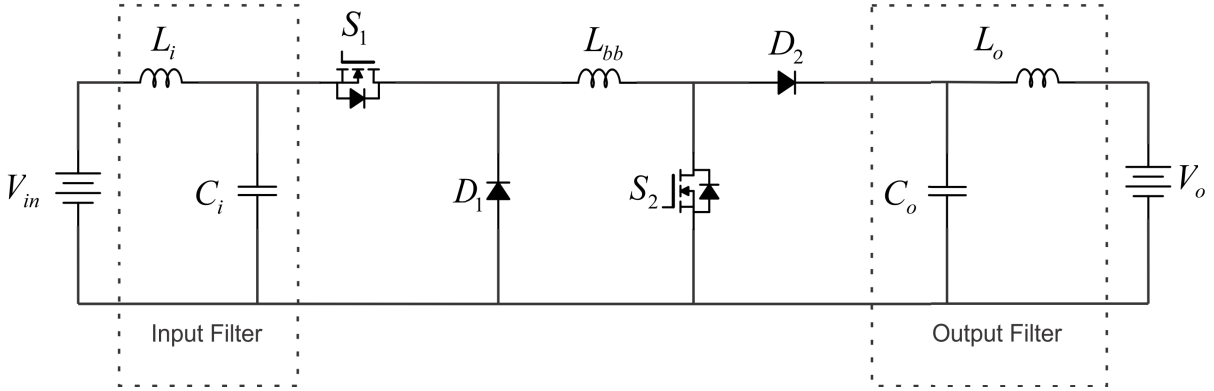
4.5 CONVERTER OPERATION WITH BATTERIES

The structure shown in Figure 4.1 is characterized by an input voltage source and a load resistor. Now, if the components of the input and output are replaced by batteries, some considerations need to be explored.

The first is avoiding pulsed currents on the batteries. These currents can not only reduce the battery lifetime, but also cause damage on it. So it is necessary to add an input filter to remove the pulsed current. On the output, the capacitor can be used as part of the filter. The Figure 4.5 brings up the converter with the batteries and the passive filters.

Also, the concept of static gain is no longer valid, once the input and output voltage is defined by the batteries, no matter which duty cycle is applied.

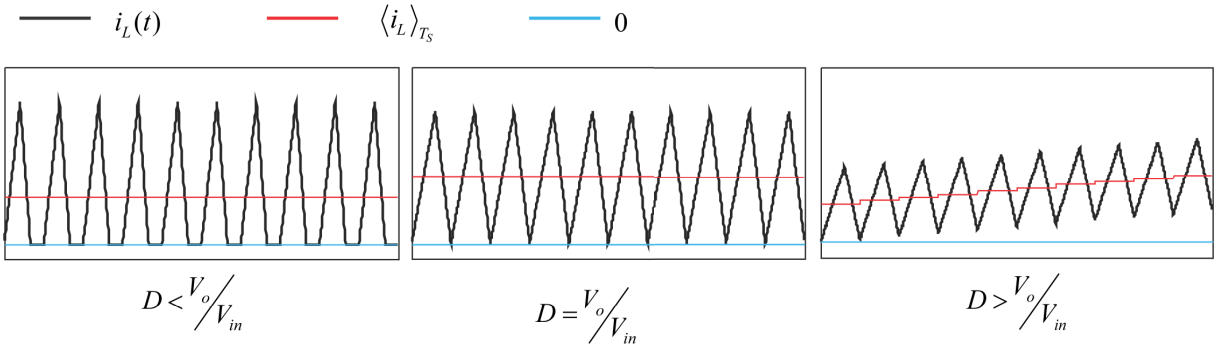
Figure 4.5 – Buck-Boost Converter with batteries



Source: Own elaborated

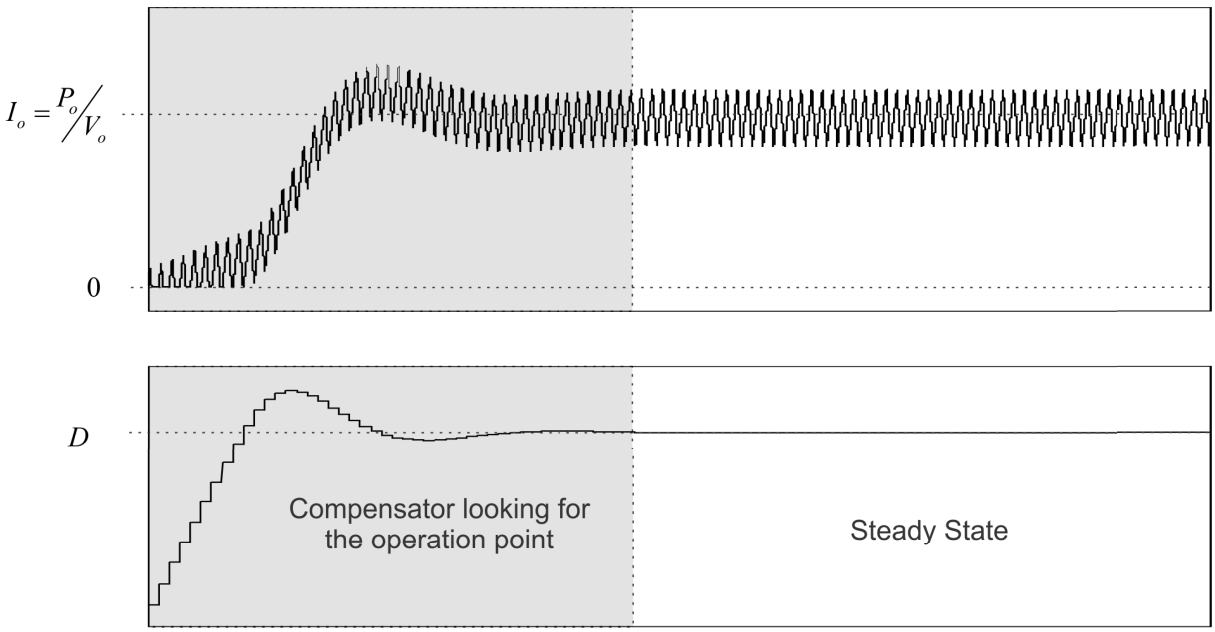
Then, a control circuit is needed. To demonstrate it, the Figure 4.6 shows what occurs with the current in different cases for the ratio of the output voltage by the input voltage, compared to the duty cycle in an open-loop system. When the duty cycle is lower than the ratio, the converter may operate in DCM condition. When it is greater, the current will be constantly increased. When it is equal, there is no change in the average value of the current.

Figure 4.6 – Open loop operation of the converter



Source: Own elaborated

Figure 4.7 – Current control in a close loop system



Source: Own elaborated

Looking at Figures 4.6 and 4.7 it becomes easy to see the importance of closed-loop control to find the steady-state operation of the converter. Without this, it would not be possible to achieve rated power.

4.5.1 Input Filter

During the interval from DT_S to T_S, the filter capacitor must absorb the average input current, once that the switches are open. So the ripple current over the capacitor can be defined as:

$$i_{C_i} = C_i \frac{dv_{C_i}}{dt} \tag{4.43}$$

$$I_{in} = C_i \frac{\Delta v_{C_i}}{(1-D)\,T_S} \tag{4.44}$$

Adjusting equation (4.44):

$$\Delta v_{C_i} = \frac{I_{in} \cdot (1-D)}{C_i \cdot f_S} \tag{4.45}$$

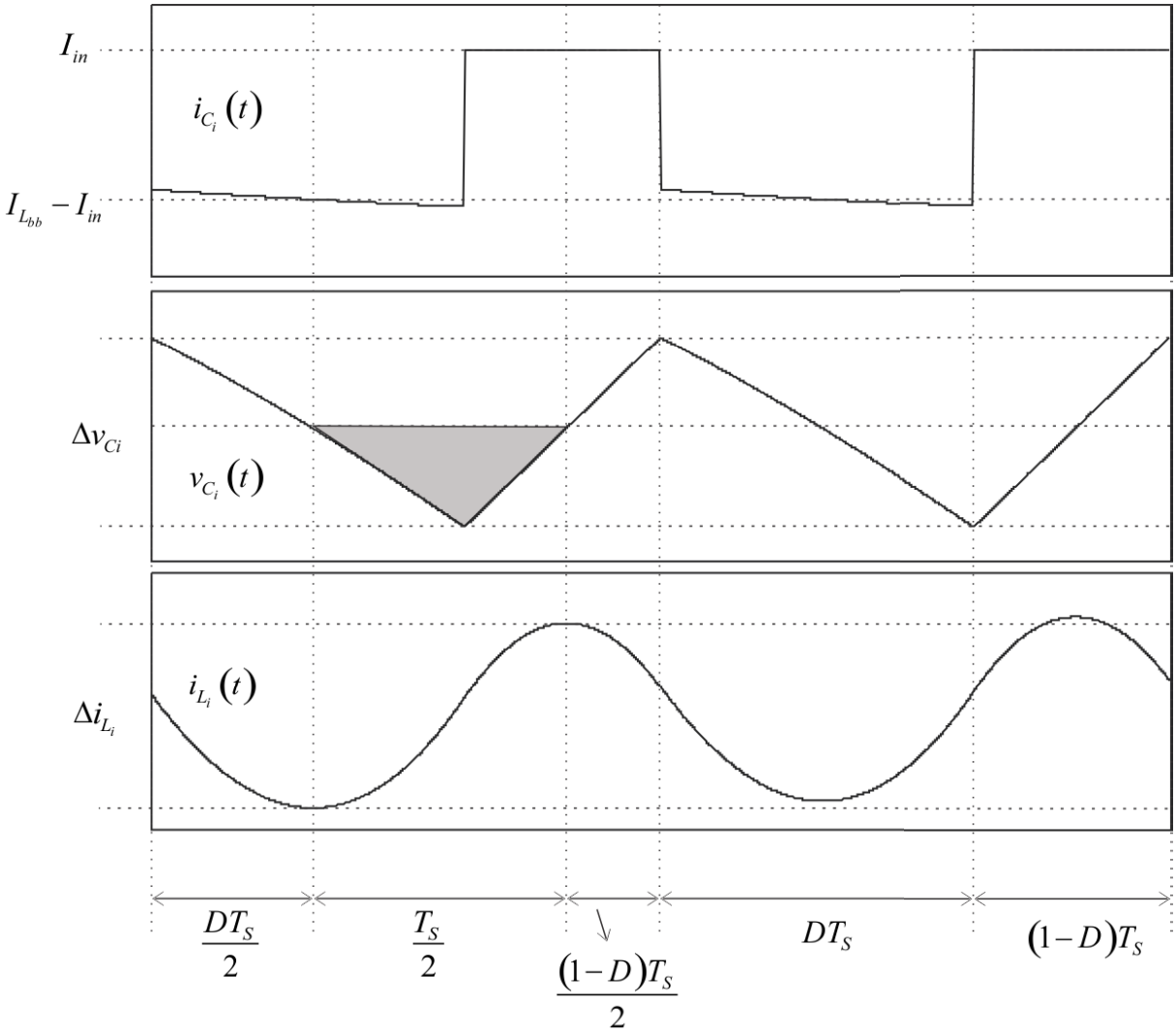
Also, the input capacitor can be sized as:

$$C_i = \frac{I_{in} \cdot (1-D)}{\Delta v_{C_i} \cdot f_S} \tag{4.46}$$

As a result of a constant voltage applied in the input, which is equal to the average value on the capacitor, the voltage over the filter inductor will be the same as

the AC component of the capacitor voltage. Figure 4.8 shows that inductor current goes from its minimum value at $\frac{DT_S}{2}$ and reaches its maximum at $DT_S + \frac{(1-D)T_S}{2}$.

Figure 4.8 – Input Filter Waveforms



Source: Own elaborated

Thus, it is possible to calculate the input ripple current:

$$v_{L_i} = L_i \frac{di_{L_i}}{dt} \tag{4.47}$$

$$L_i \cdot \Delta i_{L_i} = \int_{\frac{DT_S}{2}}^{\frac{DT_S}{2}+\frac{T_S}{2}} v_{L_i} dt \tag{4.48}$$

The integration result can be found by the area of the triangle highlighted in

Figure 4.8. Hence:

$$L_i \cdot \Delta i_{L_i} = \underbrace{\frac{T_S}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_i}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{4.49}$$

Combining equation (4.45) with (4.49), it is found:

$$\Delta i_{L_i} = \frac{I_{in} \cdot (1-D)}{8 \cdot L_i \cdot C_i \cdot f_S^2} \tag{4.50}$$

Rearranging equation (4.50) terms, the filter inductor can be sized as:

$$L_i = \frac{I_{in} \cdot (1-D)}{8 \cdot \Delta i_{L_i} \cdot C_i \cdot f_S^2} \tag{4.51}$$

4.5.2 Output Filter

The output filter capacitor is defined the same way as the output capacitor for a regular Buck-Boost converter with a resistor load. The ripple voltage is given in equation (4.16) and its sizing in equation (4.17).

$$\Delta v_{C_o} = \frac{I_o \cdot D}{C_o \cdot f_S} \tag{4.52}$$

$$C_o = \frac{I_o \cdot D}{\Delta v_{C_o} \cdot f_S} \tag{4.53}$$

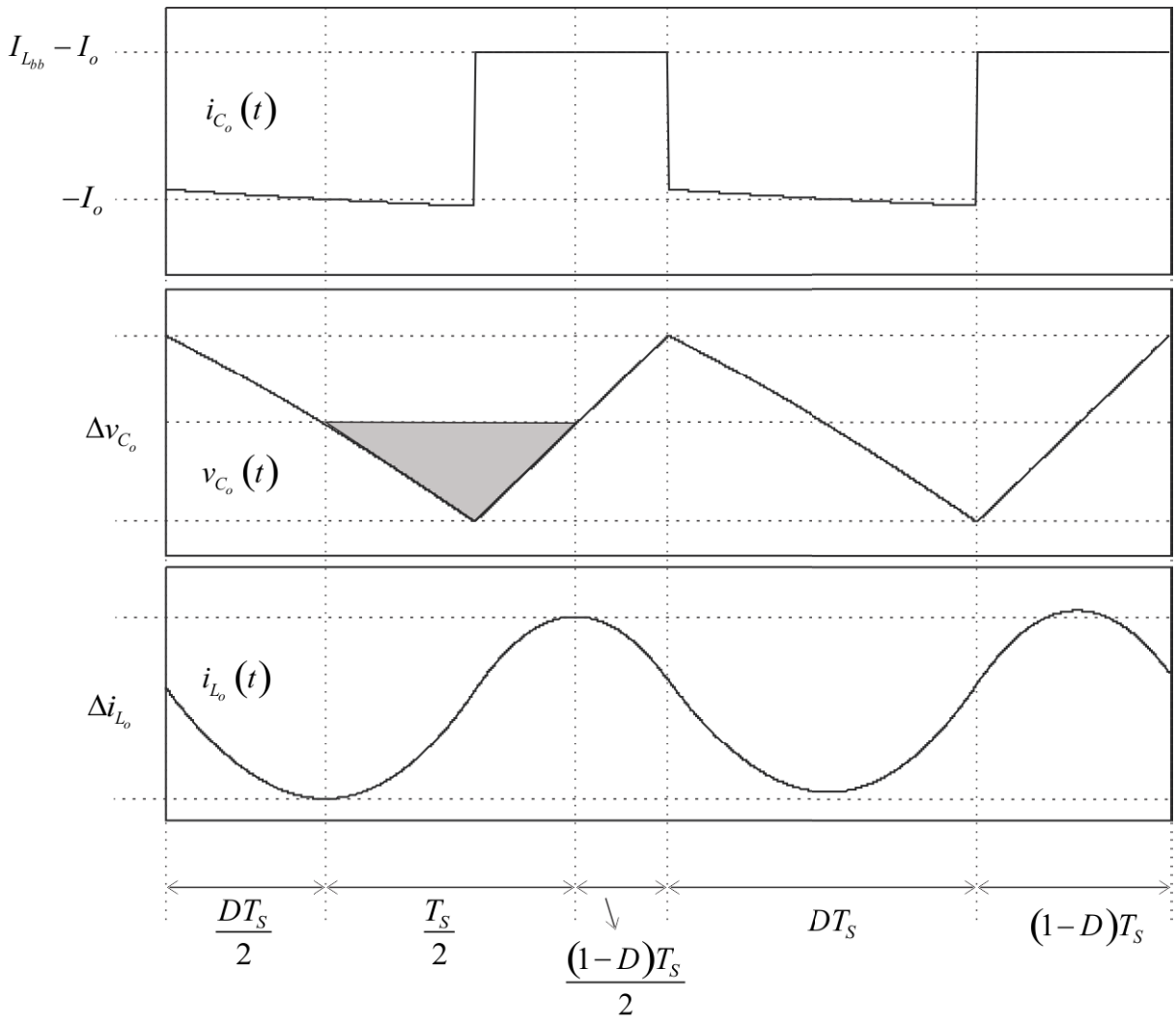
Similarly, as in input, the voltage applied on the output inductor is equal to the ripple voltage on the capacitor, once that the average voltage on the capacitor is the same as the output battery. Then:

$$v_{L_o} = L_o \frac{di_{L_o}}{dt} \tag{4.54}$$

$$L_o \cdot \Delta i_{L_o} = \int_{\frac{DT_S}{2}}^{\frac{DT_S}{2}+\frac{T_S}{2}} v_{L_o} dt \tag{4.55}$$

The integration result is equal to the area of the triangle highlighted in Figure 4.9.

Figure 4.9 – Waveforms on output filter



Source: Own elaborated

$$L_o \cdot \Delta i_{L_o} = \underbrace{\frac{T_S}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_o}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{4.56}$$

$$\Delta i_{L_o} = \frac{I_o \cdot D}{8 \cdot L_o \cdot C_o \cdot f_S^2} \tag{4.57}$$

Rearranging equation (4.57) terms, the output inductor can be sized as:

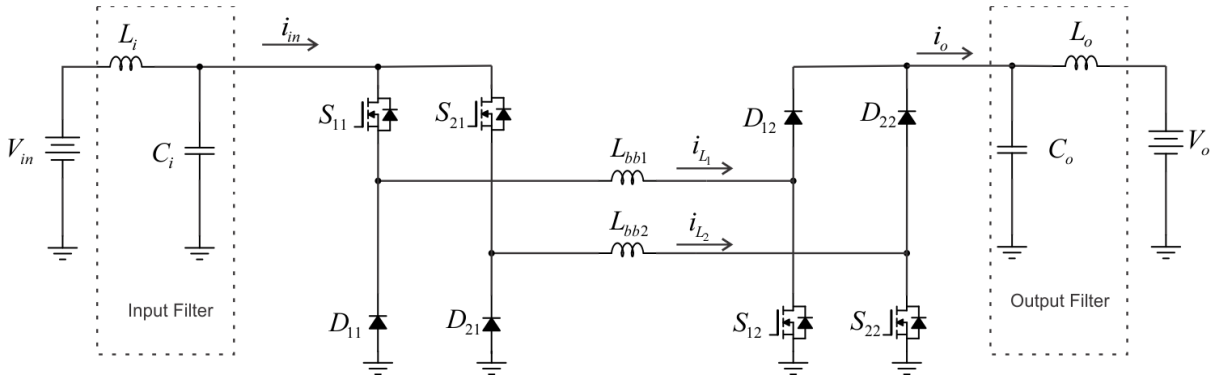
$$L_o = \frac{I_o \cdot D}{8 \cdot \Delta i_{L_o} \cdot C_o \cdot f_S^2} \tag{4.58}$$

4.6 INTERLEAVING OPERATION

Figure 4.10 shows a two-level interleaved non-inverting Buck-Boost converter. In this case, there are two different situations in which the converter will operate: (a) ON

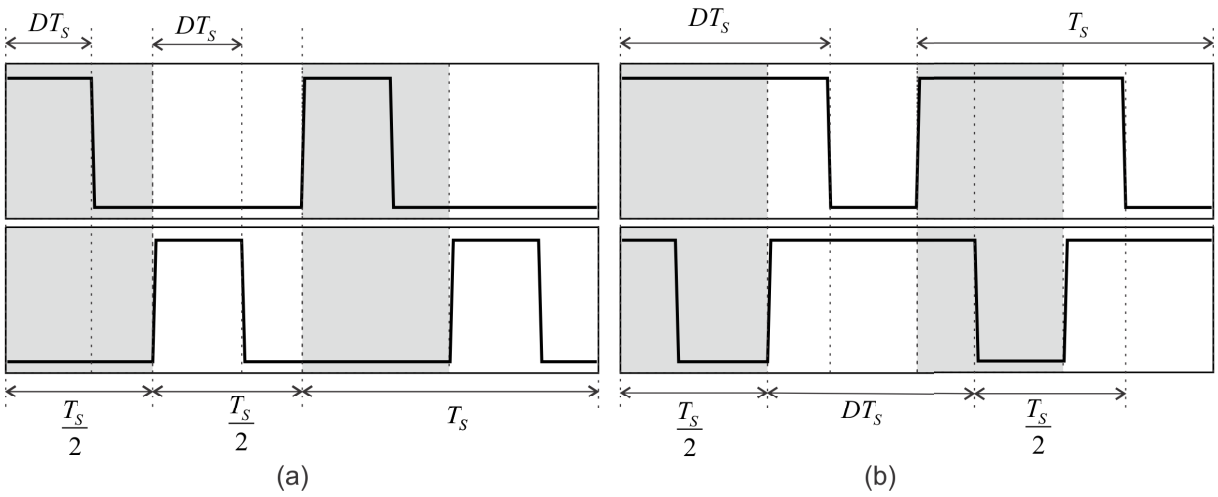
time lower than the phase shift or (b) ON time greater than the phase shift. These are shown, respectively, in Figure 4.11.

Figure 4.10 – Two level non-inverting Buck-Boost



Source: Own elaborated

Figure 4.11 – Operation modes of two level Buck-Boost converter

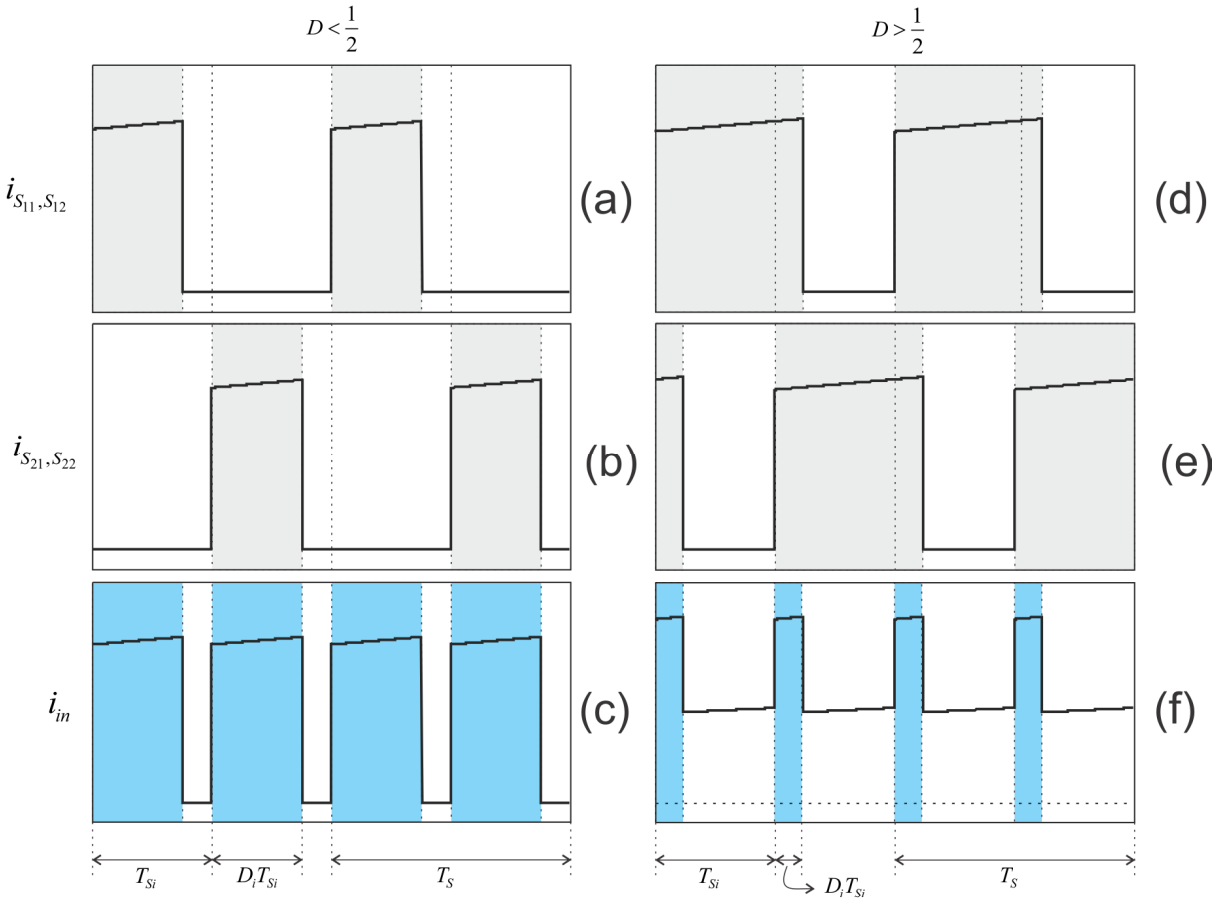


Source: Own elaborated

4.6.1 Changes in the Input and Output Current

With the interleaving technique, it is possible to reduce the ripple magnitudes in the current and in the voltage in the converter input and output. Figure 4.12 presents the input switch current of each converter and its sum, which is equal to the input current.

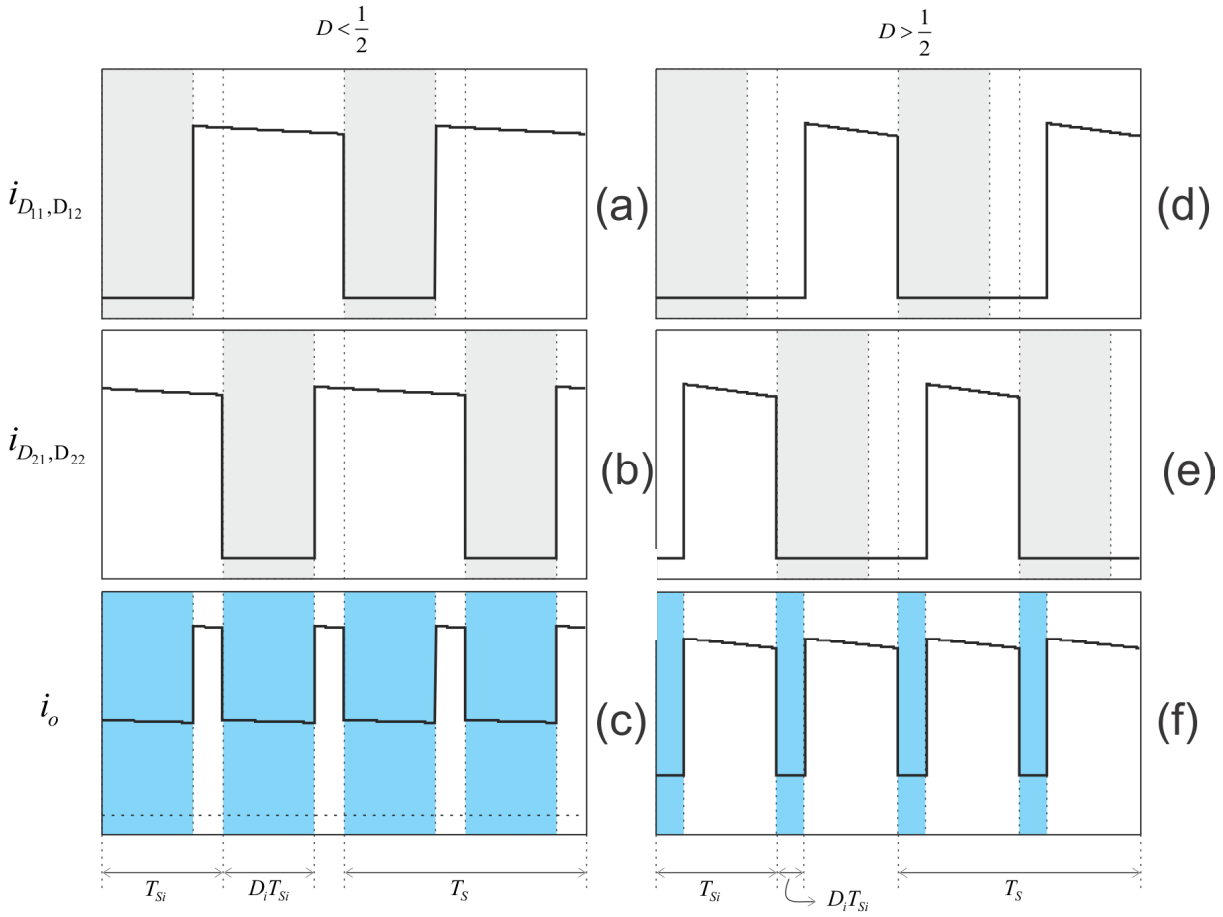
Figure 4.12 – Input current on two level Buck-Boost



Source: Own elaborated

In figure 4.13 it is presented the output current, which is the sum of each output diode.

Figure 4.13 – Output current on two level Buck-Boost



Source: Own elaborated

Therefore, it is necessary to obtain new values to define the ripple voltage and current over the filters. To achieve that, the equations defined in Appendix A are used.

4.6.2 Interleaved NIBB Input filter

The ripple voltage over the input capacitor can be calculated from:

$$i_{C_i} = C_i \frac{dv_{C_i}}{dt} \tag{4.59}$$

In a complementary interval of D_iT_{Si}, the capacitor must receive the result of the average input current subtracted of each conducting switch. Hence:

$$I_{in} - n_{on} \cdot I_{L_{bb}} = C_i \frac{\Delta v_{C_i}}{(1-D_i)\,T_{Si}} \tag{4.60}$$

$$n \cdot D \cdot I_{L_{bb}} - n_{on} \cdot I_{L_{bb}} = C_i \frac{\Delta v_{C_i}}{(1-D_i)\,T_{Si}} \tag{4.61}$$

$$I_{L_{bb}} \cdot \left(\underbrace{n \cdot D - n_{on}}_{D_i} \right) = C_i \frac{\Delta v_{C_i}}{(1 - D_i)\, T_{Si}} \tag{4.62}$$

Applying the needed algebraic manipulations, it is found:

$$\Delta v_{C_i} = \frac{I_{L_{bb}} \cdot D_i \cdot (1 - D_i)}{C_i \cdot f_S \cdot n} \tag{4.63}$$

Normalizing equation (4.63):

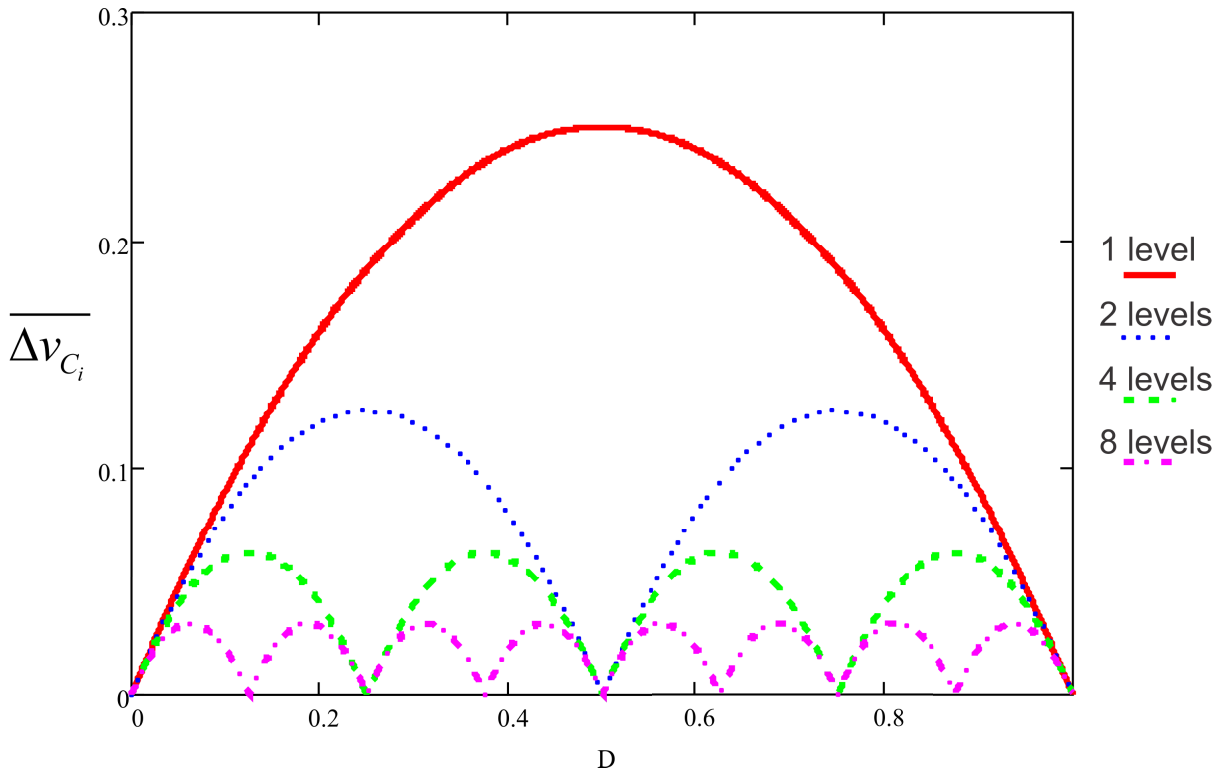
$$\overline{\Delta v_{C_i}} = \frac{C_i \cdot f_S}{I_{L_{bb}}} \cdot \Delta v_{C_i} \tag{4.64}$$

Hence:

$$\overline{\Delta v_{C_i}} = \frac{D_i \cdot (1 - D_i)}{n} \tag{4.65}$$

From equation (4.65), Figure 4.14 shows the normalized ripple voltage according to the converter operating point and the number of interleaved converters.

Figure 4.14 – Normalized ripple voltage over input capacitor



Source: Own elaborated

Maximizing equation (4.63) regarding D_i, the input capacitor can be described as:

$$C_i = \frac{I_{L_{bb}}}{4 \cdot \Delta v_{C_i} \cdot f_S \cdot n} \tag{4.66}$$

To find the ripple current over the input inductor, similarly to equation (4.56), it is used the ripple voltage over the capacitor. The difference now is the interval in which it happens, which is $T_S i$. Therefore:

$$v_{L_i} = L_e \frac{di_{L_i}}{dt} \tag{4.67}$$

$$L_i \cdot \Delta i_{L_i} = \underbrace{\frac{T_{Si}}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_i}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{4.68}$$

Adjusting equation (4.68):

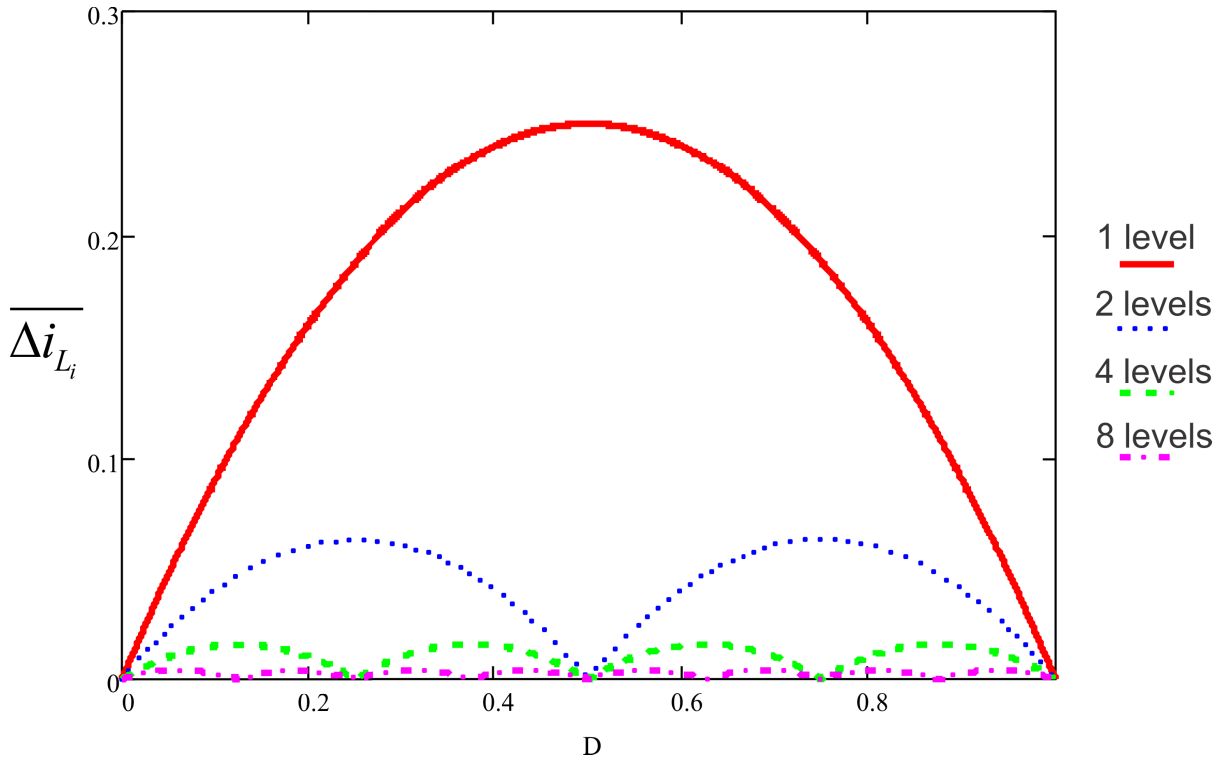
$$\Delta i_{L_i} = \frac{I_{L_{bb}} \cdot D_i \cdot (1 - D_i)}{8 \cdot L_i \cdot C_i \cdot f_S^2 \cdot n^2} \tag{4.69}$$

Normalizing equation (4.69):

$$\overline{\Delta i_{L_i}} = \frac{8 \cdot L_i \cdot C_i \cdot f_S^2}{I_{L_{bb}}} \cdot \Delta i_{L_i} \tag{4.70}$$

Figure 4.15 presents the normalized ripple current on the inductor according to the operating duty cycle and the number of interleaved converters.

Figure 4.15 – Normalized ripple current on input inductor



Source: Own elaborated

Maximizing equation (4.69) in relation of D_i, the inductor sizing can be described as:

$$L_i = \frac{I_{L_{bb}}}{32 \cdot \Delta i_{L_i} \cdot C_i \cdot f_S^2 \cdot n^2} \tag{4.71}$$

4.6.3 Interleaved NIBB Output Filter

The output capacitor can be sized from:

$$i_{C_o} = C_o \frac{dv_{C_o}}{dt} \tag{4.72}$$

In the interval from 0 to $D_i T_{Si}$, the capacitor current is the result of the average output current subtracted by the current of conducting output diodes. Then:

$$n_{off} \cdot I_{L_{bb}} - I_o = C_o \frac{\Delta v_{C_o}}{D_i T_{Si}} \tag{4.73}$$

$$(n - n_{on} - 1) \cdot I_{L_{bb}} - n \cdot (1 - D) \cdot I_{L_{bb}} = C_o \frac{\Delta v_{C_o}}{D_i T_{Si}} \tag{4.74}$$

$$I_{L_{bb}} \cdot \left(\underbrace{n \cdot D - n_{on}}_{D_i} - 1 \right) = C_o \frac{\Delta v_{C_o}}{(1 - D_i)\, T_{Si}} \tag{4.75}$$

Adjusting equation (4.75):

$$\Delta v_{C_o} = \frac{I_{L_{bb}} \cdot D_i \cdot (1 - D_i)}{C_o \cdot f_S \cdot n} \tag{4.76}$$

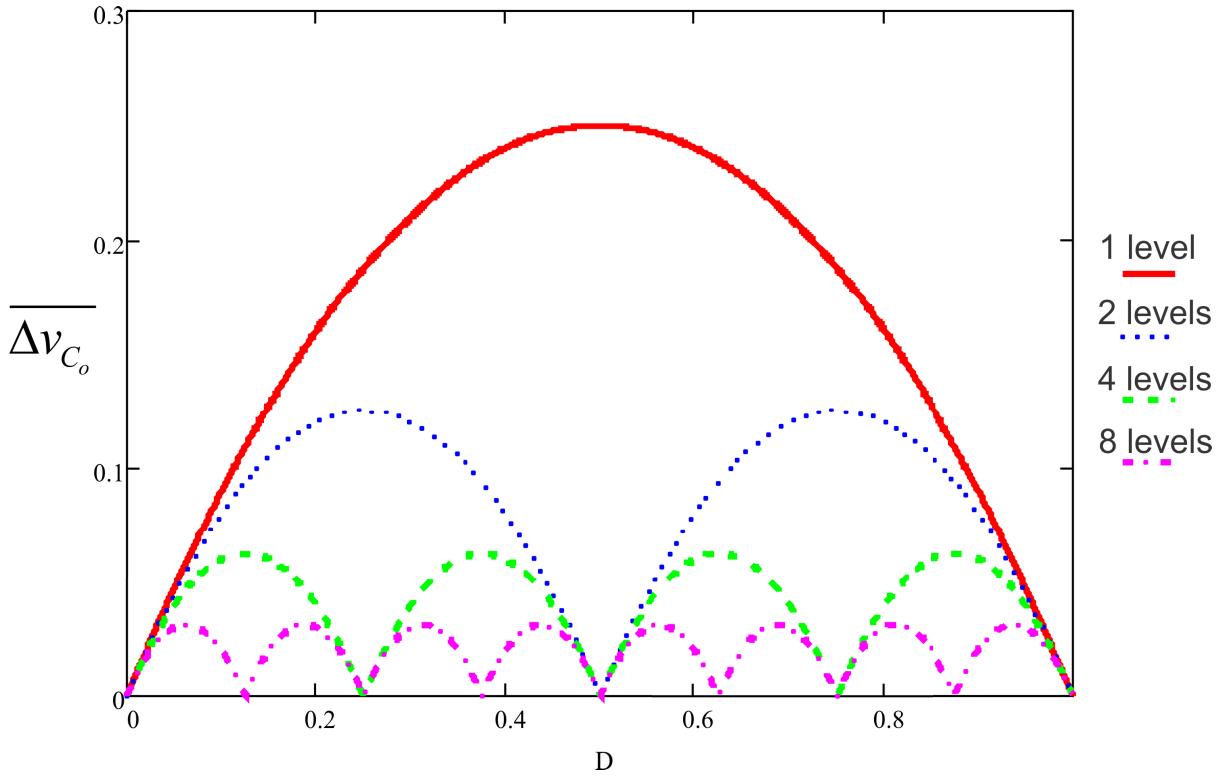
Normalizing equation (4.76):

$$\overline{\Delta v_{C_o}} = \frac{C_o \cdot f_S}{I_{L_{bb}}} \cdot \Delta v_{C_o} \tag{4.77}$$

$$\overline{\Delta v_{C_o}} = \frac{D_i \cdot (1 - D_i)}{n} \tag{4.78}$$

From equation (4.78), Figure 4.16 shows the normalized output ripple voltage according to the operating duty cycle and the number of interleaved converters.

Figure 4.16 – Normalized ripple voltage at output capacitor



Source: Own elaborated

Maximizing equation (4.76) regarding D_i, the output capacitor sizing can be expressed as:

$$C_o = \frac{I_{L_{bb}}}{4 \cdot \Delta v_{C_o} \cdot f_S \cdot n} \tag{4.79}$$

Similarly of input, the output inductor can be calculated from:

$$v_{L_o} = L_o \frac{di_{L_o}}{dt} \tag{4.80}$$

$$L_o \cdot \Delta i_{L_o} = \underbrace{\frac{T_{Si}}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_o}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{4.81}$$

Applying equation (4.76) in (4.81):

$$\Delta i_{L_o} = \frac{I_{L_{bb}} \cdot D_i \cdot (1 - D_i)}{8 \cdot L_o \cdot C_o \cdot f_S^2 \cdot n^2} \tag{4.82}$$

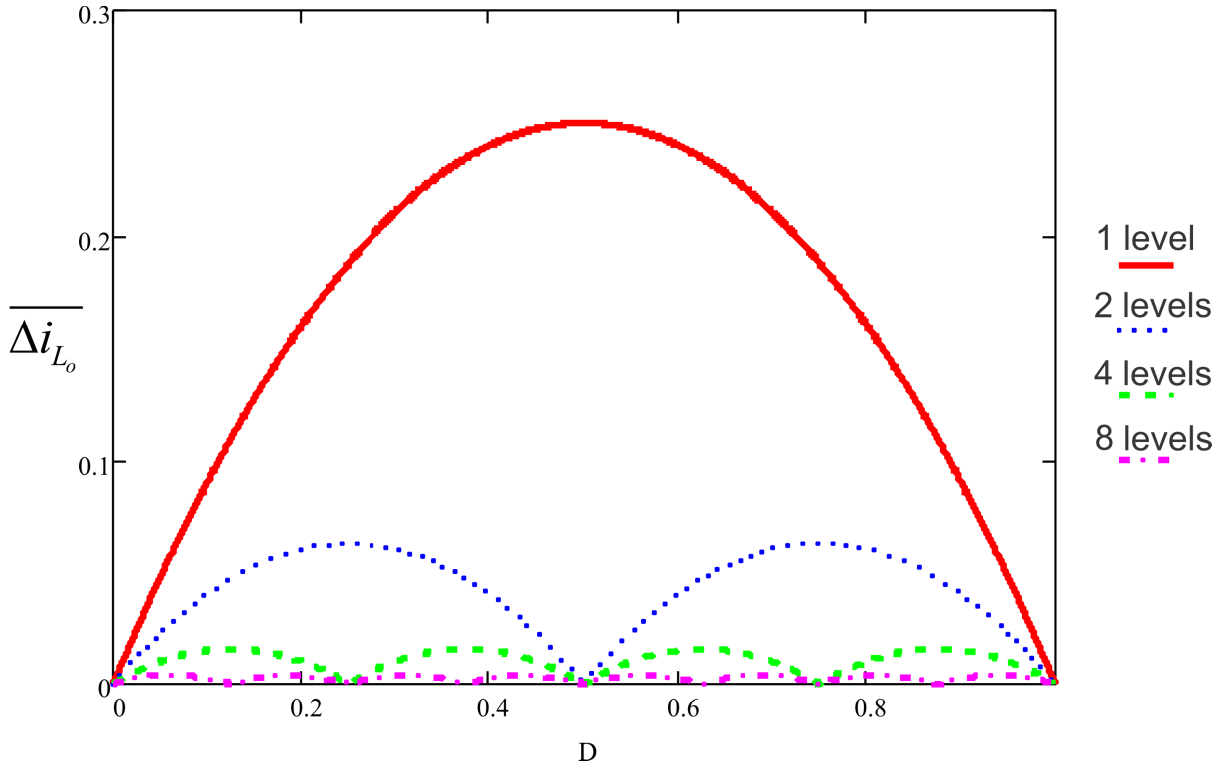
Normalizing equation (4.82):

$$\overline{\Delta i_{L_o}} = \frac{8 \cdot L_o \cdot C_o \cdot f_S^2}{I_{L_{bb}}} \cdot \Delta i_{L_o} \tag{4.83}$$

$$\overline{\Delta i_{L_o}} = \frac{D_i \cdot (1 - D_i)}{n^2} \tag{4.84}$$

From equation (4.84), Figure 4.17 presents the ripple current over the output inductor, given the operating duty cycle and the number of interleaved converters.

Figure 4.17 – Normalized ripple current in output inductor



Source: Own elaborated

Maximizing the equation (4.82) regarding D_i, the output inductor can be sized as:

$$L_o = \frac{I_{L_{bb}}}{32 \cdot \Delta i_{L_o} \cdot C_o \cdot f_S^2 \cdot n^2} \tag{4.85}$$

4.7 PARTIAL CONCLUSIONS

As seen, the Non-Inverting Buck-Boost with the same gate signal can operate as a step up and step down converter, and its operation with batteries may require filters on input and output due to its pulsed current in both terminals.

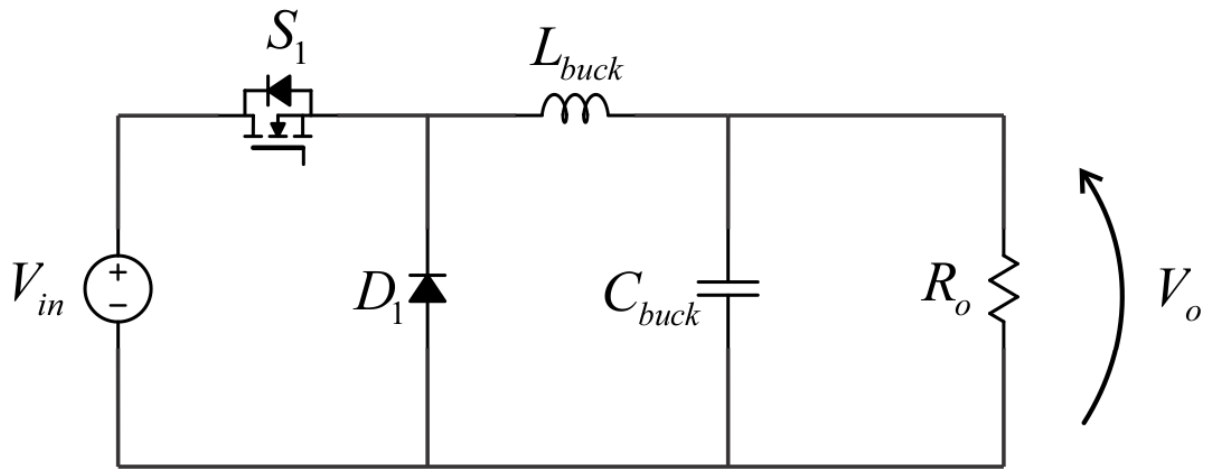
Using interleaving techniques, the oscillations of voltage and current are reduced. In addition, the resulting frequency is increased. As a consequence, the volume of the passive filters can be reduced, when compared to a single converter processing the same power.

Next, it is presented the single Buck converter, that is one converter derived from NIBB when operated with different gate signals.

5 STUDY OF BUCK CONVERTER IN CONTINUOUS CONDUCTION MODE

Among the non-isolated step-down converters, the Buck topology presents a reduced number of components. It is characterized by a voltage source in the input, a switch, a diode, an inductor, a capacitor, and the load. The last-mentioned is represented by a resistor in Figure 5.1.

Figure 5.1 – Buck Topology

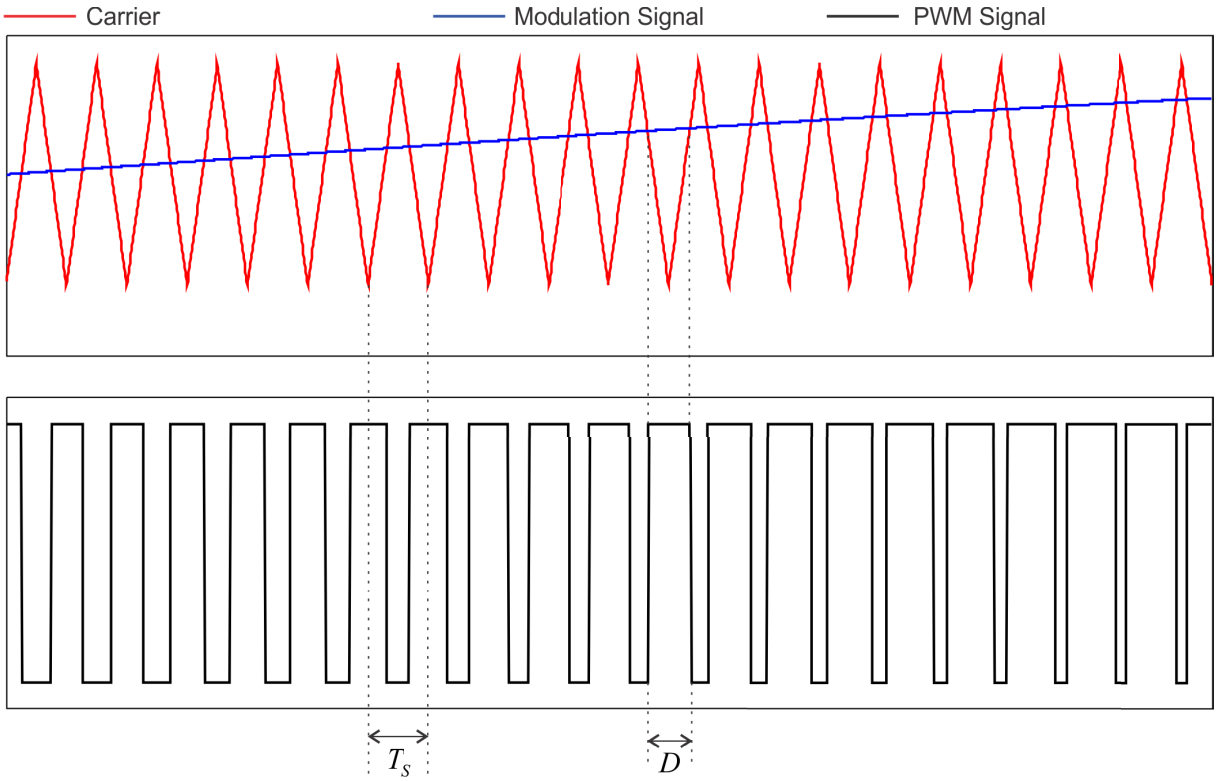


Source: Own elaborated

5.1 MODULATION

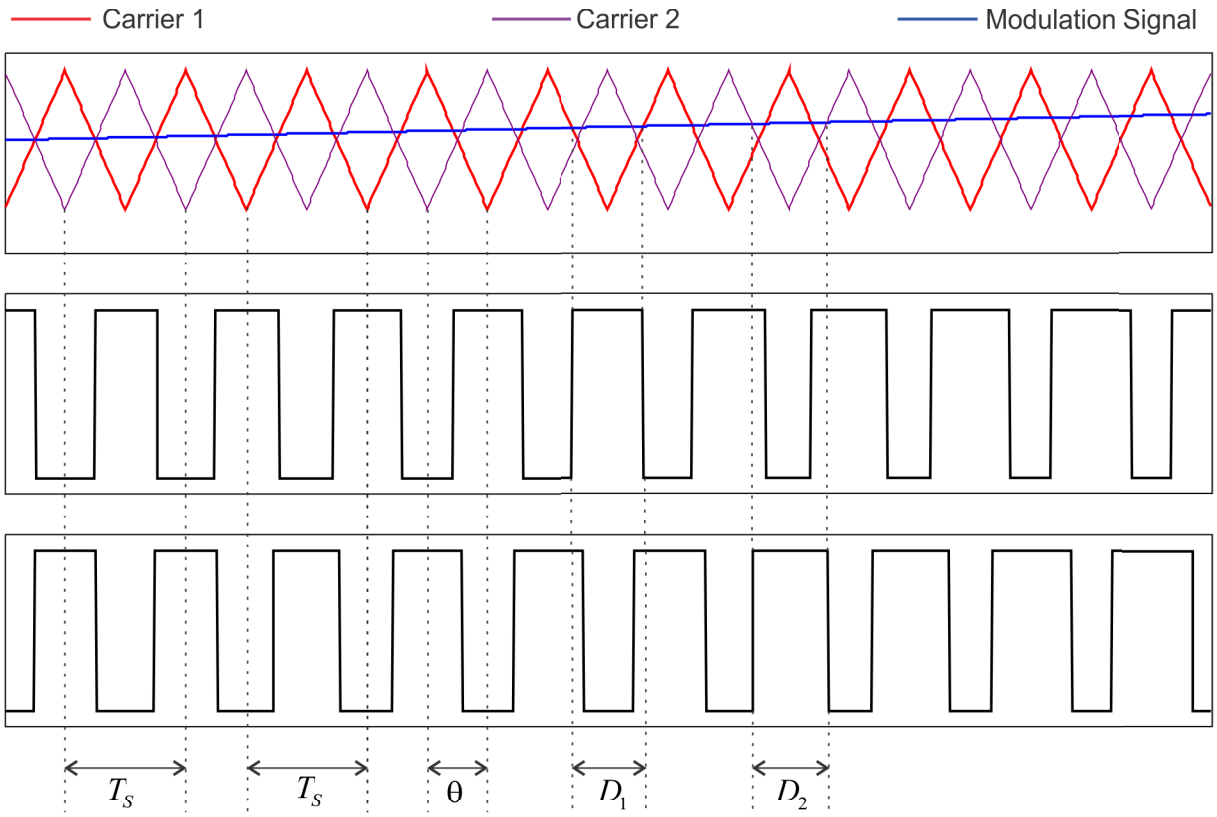
One of the modulation strategies of switched converters is based on PWM control. In other words, a triangular carrier with the desired switching frequency is compared to a modulation signal. This comparison results in the PWM pulse mentioned before and is seen in Figure 5.2. To interleaved converters, it is possible to use the phase shift between the carriers. This technique can produce the same PWM signal time-shifted, as presented in Figure 5.3.

Figure 5.2 – Modulation singnal, Carrier, and PWM Pulse



Source: Own elaborated

Figure 5.3 – PWM Pulses for 2 Interleaved converters

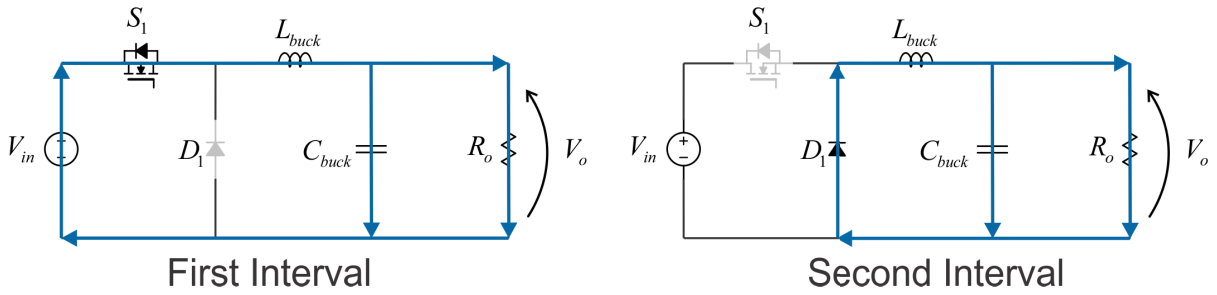


Source: Own elaborate

5.2 TOPOLOGICAL STATES

When operating in Continuous Conduction Mode (CCM), a PWM controlled converter presents two basic topological states. In the first subinterval, the switch is closed in applying a voltage across the inductor. In the second subinterval, the switch is opened because the energy stored on the inductor needs a new path to flow. So the diode creates this path. The procedure is illustrated in Figure 5.4.

Figure 5.4 – Topological States of Buck Converter

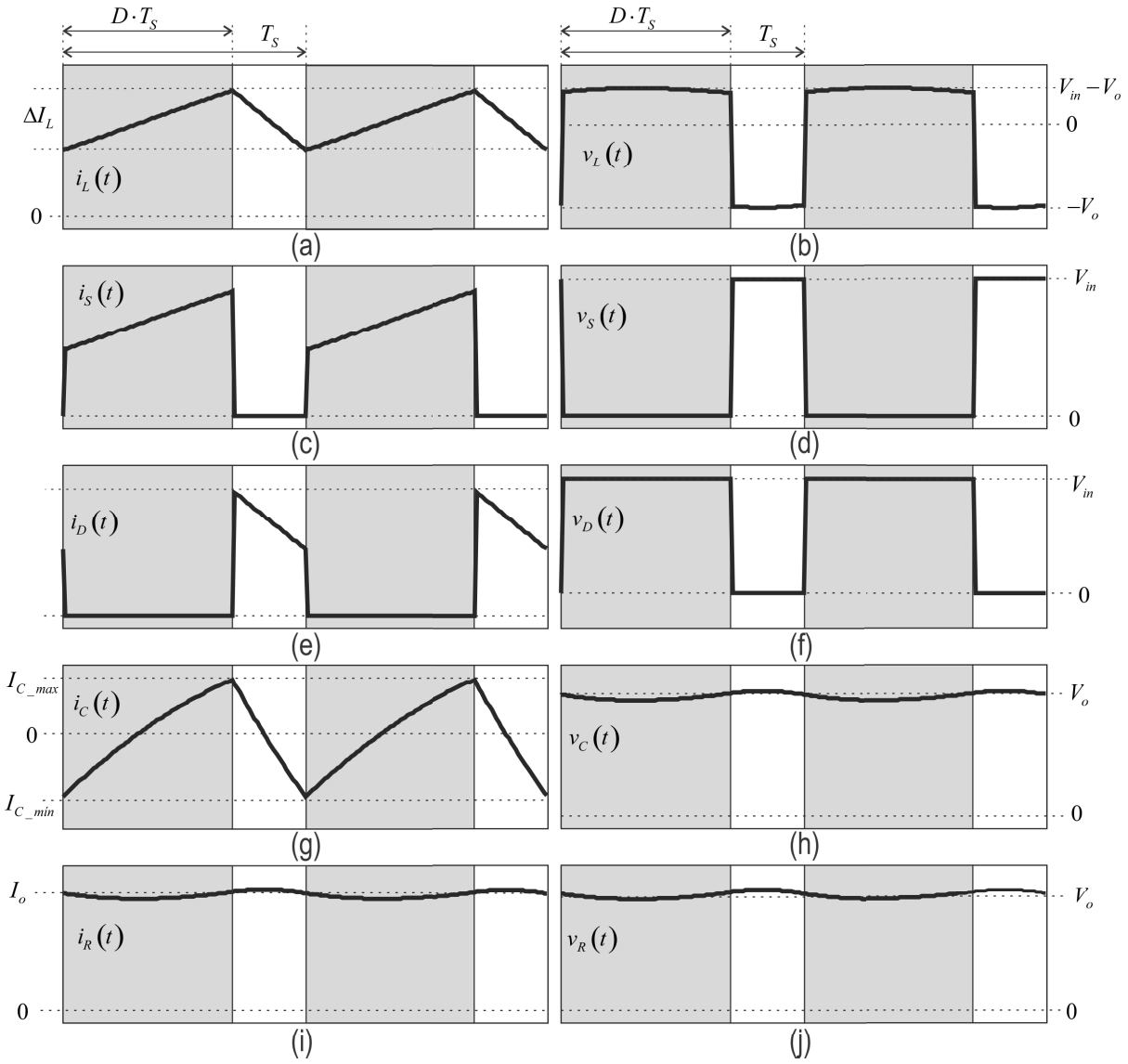


Source: Own elaborated

5.3 WAVEFORMS

Stating that the converter will operate in CCM, the waveforms of each subinterval are presented in Figure 5.5, wherein is shown: (a) current and (b) voltage on the inductor; (c) current and (d) voltage on the switch; (e) current and (f) voltage on diode; (g) current and voltage on the capacitor; (i) current and (j) voltage in the load resistor.

Figure 5.5 – Buck CCM Waveforms



Source: Own Elaborated

5.4 ALGEBRAIC ANALYSIS

In this section will be determined the algebraic equations for the voltages and currents on the components of the converter, based on the topological states.

5.4.1 Inductor

The average voltage over the inductor in a switching interval is:

$$V_{L_{buck}} = \frac{(V_{in} - V_o) \cdot D \cdot T_S + (-V_o) \cdot (1 - D) \cdot T_S}{T_S} \tag{5.1}$$

In a steady-state, the inductor does not accumulate energy. This means that all the energy stored will be transferred on the switching period. Thus:

$$V_{L_{buck}} = 0 \tag{5.2}$$

Applying (5.1) in (5.2):

$$V_{in} \cdot D = V_o \tag{5.3}$$

Similarly, the static gain is defined as:

$$\frac{V_o}{V_{in}} = D \tag{5.4}$$

Also, the instantaneous voltage across the inductor can be given by equation (5.5).

$$V_{L_{buck}} = L_{buck} \frac{di_{L_{buck}}}{dt} \tag{5.5}$$

In the first subinterval, the switch S_1 is closed, applying the following voltage:

$$V_{in} - V_o = L_{buck} \frac{di_{L_{buck}}}{dt} \tag{5.6}$$

For the first subinterval, it can be considered:

$$\frac{di_{L_{buck}}}{dt} = \frac{\Delta i_{L_{buck}}}{\Delta t} \tag{5.7}$$

Wherein:

$$\Delta t = D \cdot T_S \tag{5.8}$$

Applying (5.8) in (5.7), it is obtained:

$$\frac{di_{L_{buck}}}{dt} = \frac{\Delta i_{L_{buck}}}{D \cdot T_S} \tag{5.9}$$

Replacing (5.9) in (5.6):

$$V_{in} - V_o = L_{buck} \frac{\Delta i_{L_{buck}}}{D \cdot T_S} \tag{5.10}$$

To put in another way:

$$V_{in} - D \cdot V_{in} = L_{buck} \frac{\Delta i_{L_{buck}}}{D \cdot T_S} \tag{5.11}$$

The current ripple in the inductor is given by:

$$\Delta i_{L_{buck}} = \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{L_{buck}} \tag{5.12}$$

Rewriting the equation (5.12) as a expression for the inductor:

$$L_{buck} = \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{\Delta i_{L_{buck}}} \tag{5.13}$$

The switching frequency is the inverse of the period. With this in mind, the expression to determine the inductance value is:

$$L_{buck} = \frac{V_{in} \cdot D \cdot (1-D)}{\Delta i_{L_{buck}} \cdot f_S} \tag{5.14}$$

It is important to remember that these equations are only valid in Continuous Conduction Mode.

The average current on Buck is equal to the output current.

$$I_{L_{buck}} = I_o \tag{5.15}$$

5.4.2 Capacitor

In order to set a continuous current on the output load, the capacitor must absorb the ripple current created by the switched circuit. With that in mind, it can be concluded that the average current on the inductor will be the same as the current on the load resistor. Hence, the voltage ripple is given by:

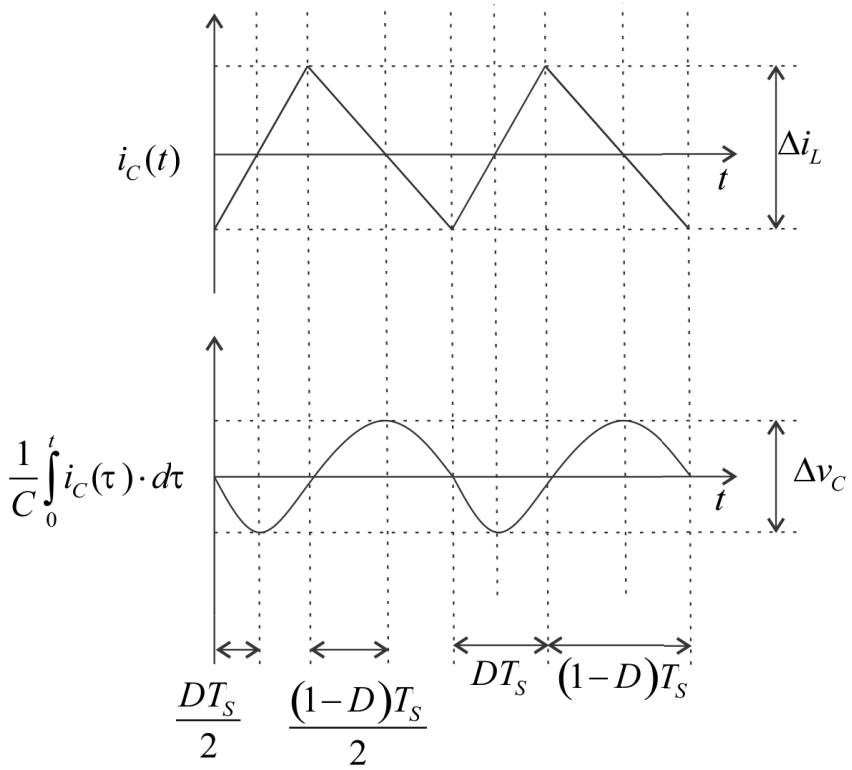
$$i_{C_{buck}} = C_{buck} \frac{dv_{C_{buck}}}{dt} \tag{5.16}$$

$$\Delta v_{C_{buck}} = \frac{1}{C_{buck}} \int i_{C_{buck}}(\tau)\, d\tau \tag{5.17}$$

Looking at Figure 5.6, it can be observed that the voltage ripple has its minimum value in the instant DT_S and reaches the maximum value at the instant $DT_S + \frac{T_S}{2}$. In that way, voltage ripple is equal to the triangle area of the capacitor current.

$$\int_{DT_S}^{DT_S+\frac{T_S}{2}} i_{C_{buck}}(\tau)\, d\tau = \underbrace{\frac{T_S}{2}}_{basis} \cdot \underbrace{\frac{\Delta i_L}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{5.18}$$

Figure 5.6 – Current ripple and Voltage ripple on the Capacitor



Source: Own Elaborated

Hence:

$$\Delta v_{C_{buck}} = \frac{\Delta i_{L_{buck}}}{8 \cdot C_{buck} \cdot f_S} \tag{5.19}$$

So the voltage ripple on the capacitor is given by:

$$\Delta v_{C_{buck}} = \frac{V_{in} \cdot D \cdot (1-D)}{8 \cdot L_{buck} \cdot C_{buck} \cdot f_S^2} \tag{5.20}$$

Rearranging the equation (5.20), the capacitor can be defined as:

$$C_{buck} = \frac{V_{in} \cdot D \cdot (1-D)}{8 \cdot L_{buck} \cdot \Delta v_{C_{buck}} \cdot f_S^2} \tag{5.21}$$

5.4.3 Switch

The switch current presented in the first subinterval is equal to the inductor current. In the second subinterval, the switch current goes to zero. This behavior can be seen in Figure 5.5 (c).

$$I_S = \frac{1}{T_S} \int_0^{T_S} i_S(t) \cdot dt \tag{5.22}$$

$$I_S = \frac{1}{T_S} \int_0^{DT_S} i_{L_{buck}}(t) \cdot dt \tag{5.23}$$

The expression which define the inductor current on the first subinterval is given by:

$$i_{L_{buck}}(t) = I_{L_min} + \frac{V_{in} \cdot (1-D)}{L_{buck}} \cdot t \tag{5.24}$$

Wherein:

$$I_{L_min} = I_{L_{buck}} - \frac{\Delta i_{L_{buck}}}{2} \tag{5.25}$$

Knowing that:

$$I_{L_{buck}} = \frac{V_o}{R_o} = \frac{V_{in} \cdot D}{R_o} \tag{5.26}$$

Applying (5.26) and (5.13) in (5.25):

$$I_{L_min} = \frac{V_{in} \cdot D}{R_o} - \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} \tag{5.27}$$

Hence, replacing (5.27) in (5.24):

$$i_{L_{buck}}(t) = \frac{V_{in} \cdot D}{R_o} - \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} + \frac{V_{in} \cdot (1-D)}{L_{buck}} \cdot t \tag{5.28}$$

Solving (5.23) with the obtained equation (5.28):

$$\begin{aligned} I_S = {} & \tfrac{1}{T_S} \int_0^{DT_S} \left[\tfrac{V_{in} \cdot D}{R_o} - \tfrac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} \right] \cdot dt + \\ & + \tfrac{1}{T_S} \int_0^{DT_S} \left[\tfrac{V_{in} \cdot (1-D)}{L_{buck}} \cdot t \right] \cdot dt \end{aligned} \tag{5.29}$$

So:

$$\begin{aligned} I_S = {} & \left[\tfrac{V_{in} \cdot D^2}{R_o} - \tfrac{V_{in} \cdot D^2 \cdot (1-D) \cdot T_S}{2L_{buck}} \right] + \\ & + \tfrac{V_{in} \cdot (1-D) \cdot D^2 \cdot T_S}{2L_{buck}} \end{aligned} \tag{5.30}$$

Rearranging the equation (5.30):

$$I_S = \frac{V_{in} \cdot D^2}{R_o} \tag{5.31}$$

To calculate the RMS current, it is used the equation (5.32).

$$I_{S_ef} = \sqrt{\int_0^{T_S} \frac{1}{T_S} [i_S(t)]^2 \cdot dt} \tag{5.32}$$

Similarly to the average current on the switch, the RMS switch current is calculated as:

$$I_{S_ef} = \sqrt{\int_0^{DT_S} \frac{1}{T_S}[i_{L_{buck}}(t)]^2 \cdot dt} \tag{5.33}$$

Applying (5.28) in (5.33), it is found:

$$I_{S_ef} = \sqrt{\int_0^{DT_S} \frac{1}{T_S}\left[\begin{array}{l}\frac{V_{in}\cdot D}{R_o} - \frac{V_{in}\cdot D\cdot(1-D)\cdot T_S}{2L_{buck}} + \\ +\frac{V_{in}\cdot(1-D)}{L_{buck}}\cdot t\end{array}\right]^2 \cdot dt} \tag{5.34}$$

Solving the expression (5.34), it is achieved:

$$I_{S_ef} = \sqrt{\frac{D^3 \cdot {V_{in}}^2 \cdot \left(\begin{array}{l} D^2\cdot R_o\cdot T_S - 2\cdot D\cdot R_o^2\cdot T_S^2 + \\ +12\cdot {L_{buck}}^2 + R_o^2\cdot T_S^2\end{array}\right)}{12\cdot {L_{buck}}^2\cdot R_o^2}} \tag{5.35}$$

Looking at Figure 5.5 (d), it is possible to determine the maximum voltage applied on the switch:

$$V_{S_max} = V_{in} \tag{5.36}$$

5.4.4 Diode

The diode current which is shown in Figure 5.5 (e) is defined equal the current on the inductor in the second subinterval.

$$I_D = \frac{1}{T_S}\int_0^{T_S} i_D(t)\cdot dt \tag{5.37}$$

Then:

$$I_D = \frac{1}{T_S}\int_{DT_S}^{T_S} i_{L_{buck}}(t)\cdot dt \tag{5.38}$$

The function that represents the inductor current in the second subinterval is defined as:

$$i_{L_{buck}}(t) = I_{L_max} - \frac{V_o}{L_{buck}}\cdot(t - D\cdot T_S) \tag{5.39}$$

Or:

$$i_L(t) = I_{L_max} - \frac{V_{in}\cdot D}{L_{buck}}\cdot(t - D\cdot T_S) \tag{5.40}$$

Knowing that:

$$I_{L_max} = I_{L_{buck}} + \frac{\Delta i_{L_{buck}}}{2} \tag{5.41}$$

Applying (5.26) and (5.13) in (5.41):

$$I_{L_max} = \frac{V_{in} \cdot D}{R_o} + \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} \tag{5.42}$$

Replacing (5.42) in (5.40), it is lead to:

$$i_{L_{buck}}(t) = \frac{V_{in} \cdot D}{R_o} + \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} - \frac{V_{in} \cdot D}{L_{buck}} \cdot (t - D \cdot T_S) \tag{5.43}$$

So the average diode current can be calculated by:

$$\begin{aligned} I_D = {} & \tfrac{1}{T_S} \int_{DT_S}^{T_S} \tfrac{V_{in} \cdot D}{R_o} \cdot dt + \tfrac{1}{T_S} \int_{DT_S}^{T_S} \tfrac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} \cdot dt + \\ & + \tfrac{1}{T_S} \int_{DT_S}^{T_S} \tfrac{-V_{in} \cdot D}{L_{buck}} \cdot (t - D \cdot T_S) \cdot dt \end{aligned} \tag{5.44}$$

Solving the equation (5.44) and performing algebraic manipulation, the diode current is equal to:

$$I_D = \frac{V_{in} \cdot D \cdot (1-D)}{R_o} \tag{5.45}$$

With the equation (5.43), the RMS current in the diode can be determined as:

$$I_{D_ef} = \sqrt{\int_{DT_S}^{T_S} \frac{1}{T_S} [i_{L_{buck}}(t)]^2 \cdot dt} \tag{5.46}$$

Replacing (5.43) in (5.46). Hence:

$$I_{D_ef} = \sqrt{\int_{DT_S}^{T_S} \frac{1}{T_S} \left[\begin{array}{l} \frac{V_{in} \cdot D}{R_o} + \frac{V_{in} \cdot D \cdot (1-D) \cdot T_S}{2L_{buck}} + \\ -\frac{V_{in} \cdot D}{L_{buck}} \cdot (t - D \cdot T_S) \end{array} \right]^2 \cdot dt} \tag{5.47}$$

Solving the equation (5.47):

$$I_{D_ef} = \frac{D \cdot V_{in}}{L \cdot R_o} \sqrt{\frac{(1-D) \left(\begin{array}{l} D^2 \cdot R_o^2 \cdot T_S^2 - 2 \cdot D \cdot R_o^2 \cdot T_S^2 + \\ +12 \cdot {L_{buck}}^2 + R_o^2 \cdot T_S^2 \end{array} \right)}{12}} \tag{5.48}$$

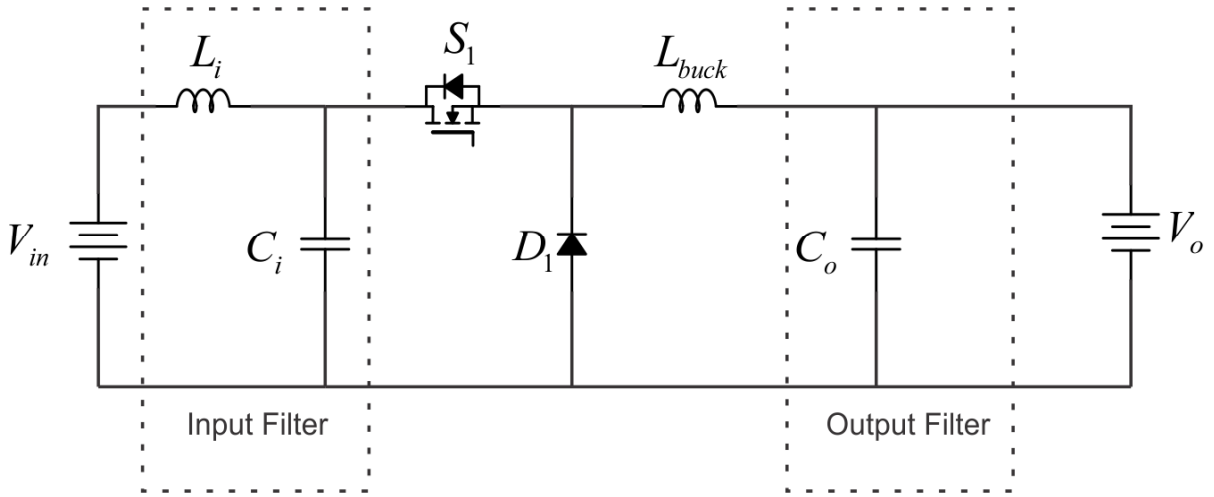
When the diode is blocked, the voltage across its terminals is equal to the input voltage.

$$V_{D_max} = V_{in} \tag{5.49}$$

5.5 CONVERTER OPERATION WITH BATTERIES

As seen in Figure 5.5, the Buck is characterized as a DC-DC converter with a pulsed current in the input and DC current on the output. In order to avoid high-frequency currents in the batteries, an input filter is required. The schematic is represented in Figure 5.7.

Figure 5.7 – Buck Converter with Batteries



Source: Own elaborated

Also, a compensator must be designed to find the converter operating point, once the concept of static gain is no longer valid.

5.5.1 Buck Input Filter

The input filter will absorb the ripple current, extracted by the converter, and extract the average current on the switching frequency. The following equations of the Buck Converter must be considered when the losses are neglected:

$$P_{in} = P_o \tag{5.50}$$

Hence:

$$V_{in} \cdot I_{in} = V_o \cdot I_o \tag{5.51}$$

$$V_{in} \cdot I_{in} = V_{in} \cdot D \cdot I_o \tag{5.52}$$

$$I_{in} = D \cdot I_o \tag{5.53}$$

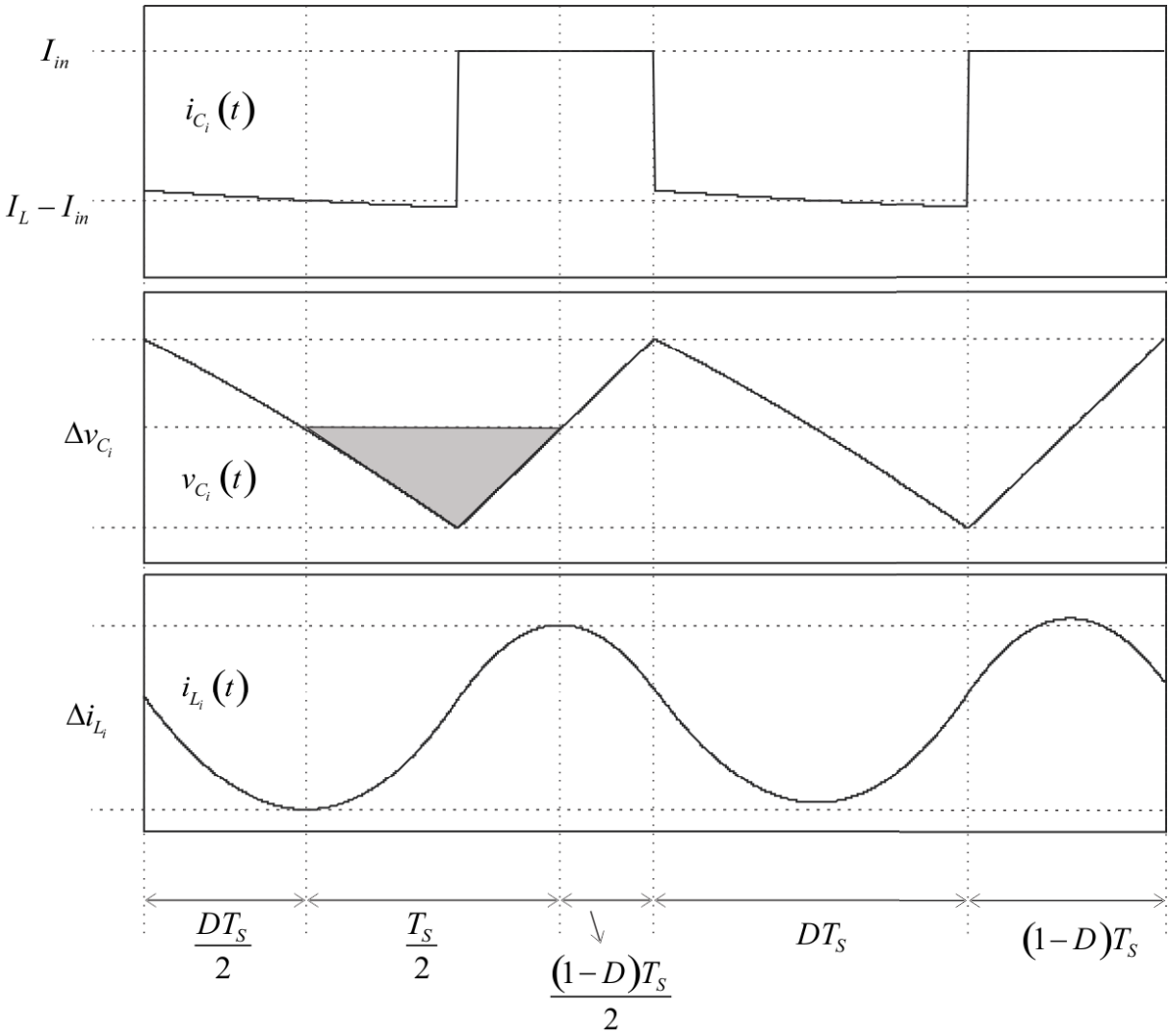
The equation (5.53) shows the expression of the average input current in the converter. When the switch is open, the capacitor current will be the average input current. It can be seen in Figure 5.8. The current $i_{C_e}(t)$ is the current on the capacitor. In order to obtain the presented waveforms, the input inductor must be designed to significantly reduce the ripple of input current.

Therefore, the voltage ripple on the capacitor can be defined from:

$$C_i \cdot \frac{dv_{C_i}}{dt} = I_{in} \tag{5.54}$$

$$C_i \cdot \frac{dv_{C_i}}{dt} = I_o \cdot D \tag{5.55}$$

Figure 5.8 – Input Filter Waveforms



Source: Own elaborated

Therefore:

$$C_i \cdot \frac{\Delta v_{C_i}}{\Delta t} = I_o \cdot D \tag{5.56}$$

$$C_i \cdot \frac{\Delta v_{C_i}}{(1-D) \cdot T_S} = I_o \cdot D \tag{5.57}$$

Adjusting the equation (5.57), it is obtained the voltage ripple across the capacitor as:

$$\Delta v_{C_i} = \frac{I_o \cdot D \cdot (1-D)}{C_e \cdot f_S} \tag{5.58}$$

Also the capacitor can be sized as:

$$C_i = \frac{I_o \cdot D \cdot (1-D)}{\Delta v_{C_i} \cdot f_S} \tag{5.59}$$

The inductor voltage waveform can be described as:

$$v_{L_i} = L_i \frac{di_{L_i}}{dt} \tag{5.60}$$

$$L_i \cdot \Delta i_{L_i} = \int v_{L_i}(t) \cdot dt \tag{5.61}$$

Considering that the average voltage across the capacitor is equal to the voltage in the input, so the voltage across the inductor is equal to the ripple voltage on the capacitor.The ripple current goes from its minimum value at $DT_S/2$ to its maximum value at $DT_S/2 + T_s/2$, as presented in Figure 5.8. Its value can be defined as the result of the differential equation:

$$L_i \cdot \Delta i_{L_i} = \int_{DT_S}^{DT_S + \frac{T_S}{2}} \Delta v_{C_i}(t) \cdot dt \tag{5.62}$$

The integral result is equal to the area filled below the average value on the capacitor voltage ripple. Hence:

$$\int_{DT_S}^{DT_S + \frac{T_S}{2}} \Delta v_{C_i}(t) \cdot dt = \underbrace{\frac{T_S}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_i}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{5.63}$$

Therefore, the ripple current on the inductor can be defined as:

$$\Delta i_{L_i} = \frac{\Delta v_{C_i}}{8 \cdot L_i \cdot f_S} \tag{5.64}$$

Or:

$$\Delta i_{L_i} = \frac{I_o \cdot D \cdot (1 - D)}{8 \cdot L_i \cdot C_i \cdot f_S^2} \tag{5.65}$$

Adjusting the equation terms (5.65), the inductor can be sized as:

$$L_i = \frac{I_o \cdot D \cdot (1 - D)}{8 \cdot C_i \cdot \Delta i_{L_i} \cdot f_S^2} \tag{5.66}$$

5.5.2 Output Filter

The output capacitor is the only element required to filter the AC currents from Buck inductors. It can be described as the customary Buck capacitor presented in equations (5.20) and (5.21).

$$\Delta v_{C_o} = \frac{V_{in} \cdot D \cdot (1 - D)}{8 \cdot L_{buck} \cdot C_o \cdot f_S^2} \tag{5.67}$$

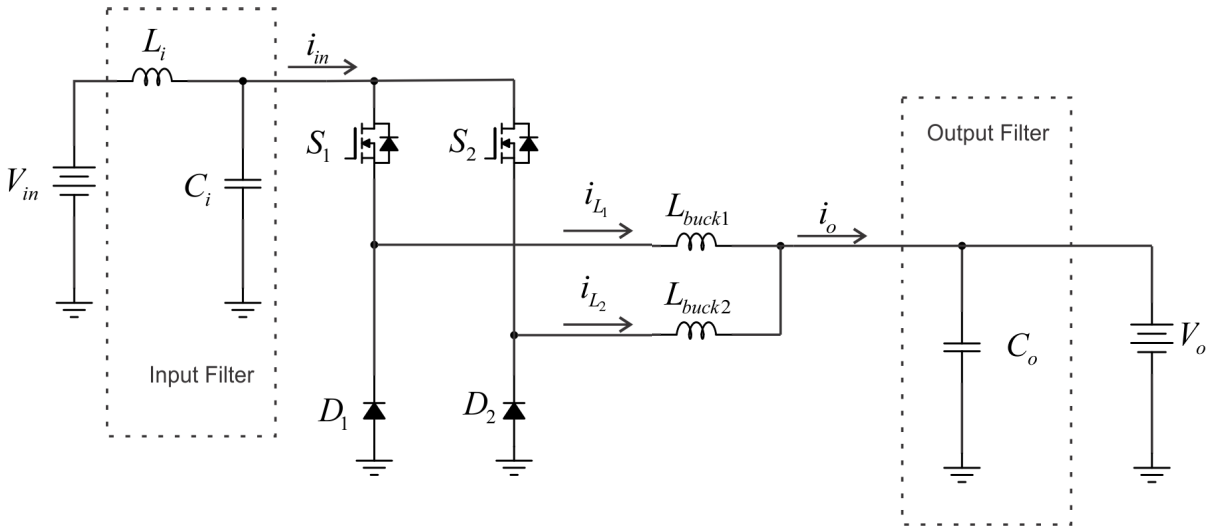
$$C_o = \frac{V_{in} \cdot D \cdot (1 - D)}{8 \cdot L_{buck} \cdot \Delta v_{C_o} \cdot f_S^2} \tag{5.68}$$

The main function of the filter is to provide a DC current component for the batteries. The series impedance of the batteries will force the AC current flow through the capacitor, similarly to the resistive load.

5.6 INTERLEAVING OPERATION

In Figure 5.9, it is presented a two-level Buck converter to charge batteries. Also, it is shown the two filter structures: in the input and on the output. As it was mentioned before, there are some possibles scenarios: the duty cycle smaller than the phase shift of the carrier signals, or greater. This can be seen in Figure 5.10.

Figure 5.9 – Two Level Buck Topology



Source: Own elaborated

The phase shift of the converter will be:

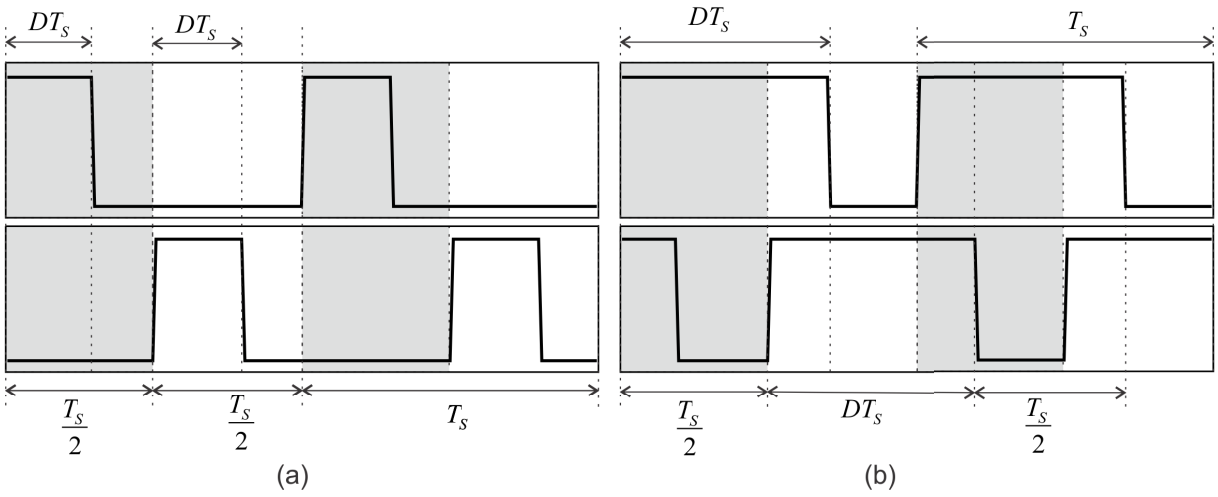
$$\theta = \frac{360}{2} = 180 \tag{5.69}$$

It can also be represented on a time scale as:

$$t_\theta = \frac{180}{360} \cdot T_S = \frac{T_S}{2} \tag{5.70}$$

Wherein T_S is the switching period:

Figure 5.10 – Operation Mode of Two Level Buck



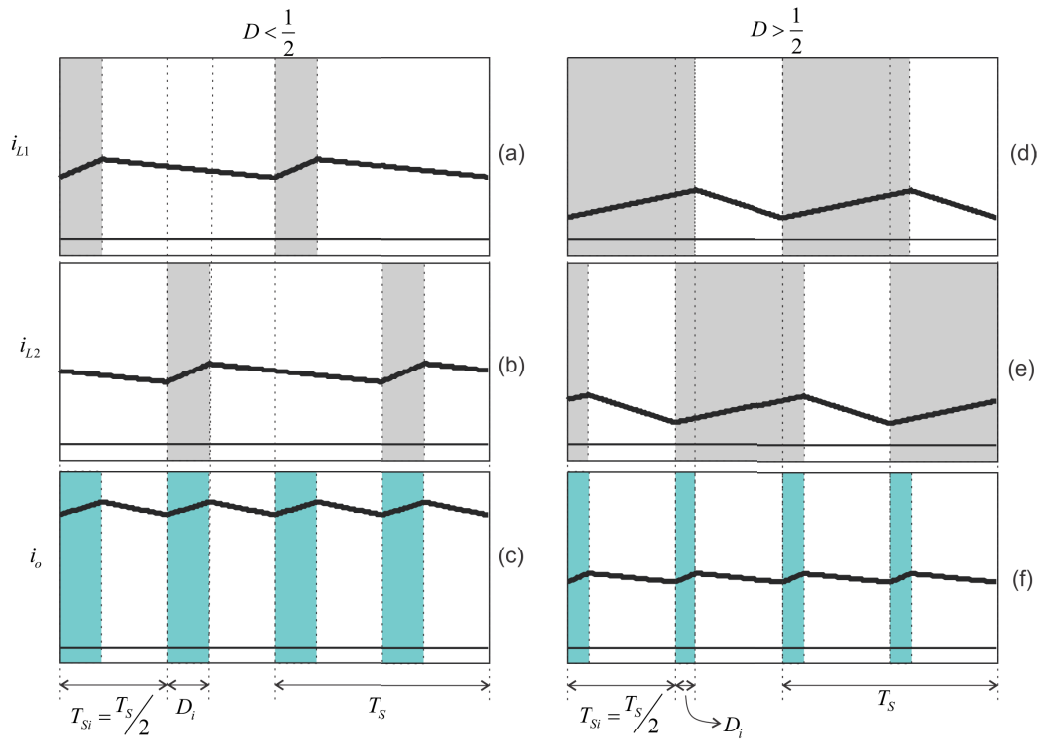
Source: Own elaborated

5.6.1 Changes in the Input and Output Current

As seen in the previous chapter, the interleaving operation modifies the input and output waveforms. Using Appendix A, it is defined as the new ripple in the input filter.

Figure 5.11 presents the new waveforms of output current for a two-level interleaved Buck converter.

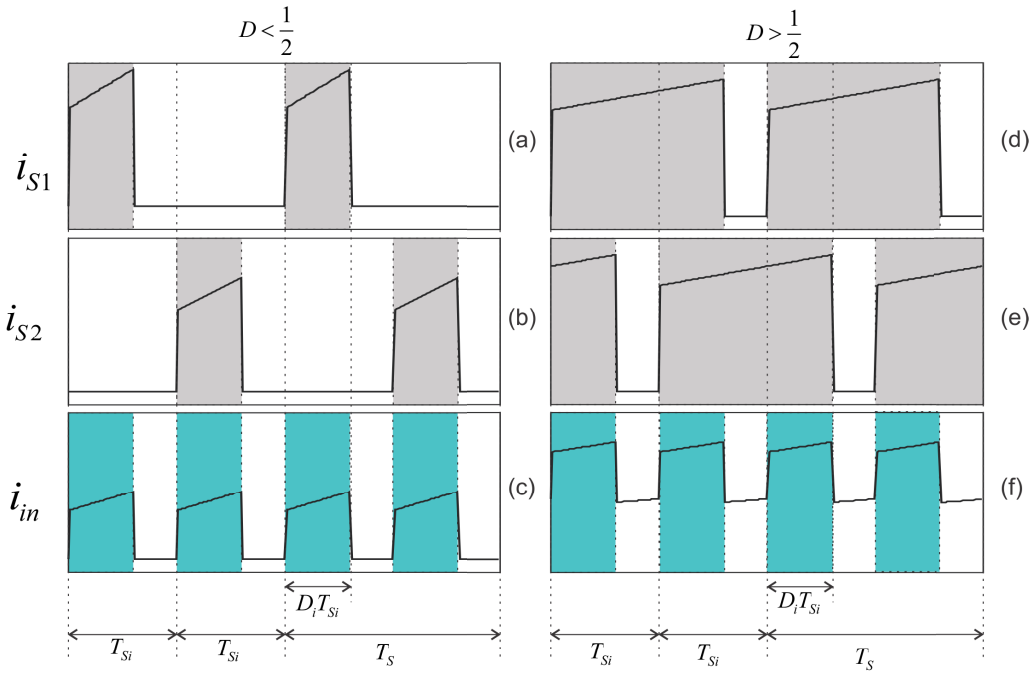
Figure 5.11 – Output current of Two Interleaved Buck Converters



Source: Own Elaborated

Similar changes will occur in the input current. When the duty cycle is smaller than half, one switch will be open during each T_{Si} subinterval. So the total input current will periodically reach zero. If it is greater than half, there will be one switch closed each subinterval T_{Si}. In this case, the total input current won't be zeroed.

Figure 5.12 – Input Currents of 2 Level Interleaved Buck



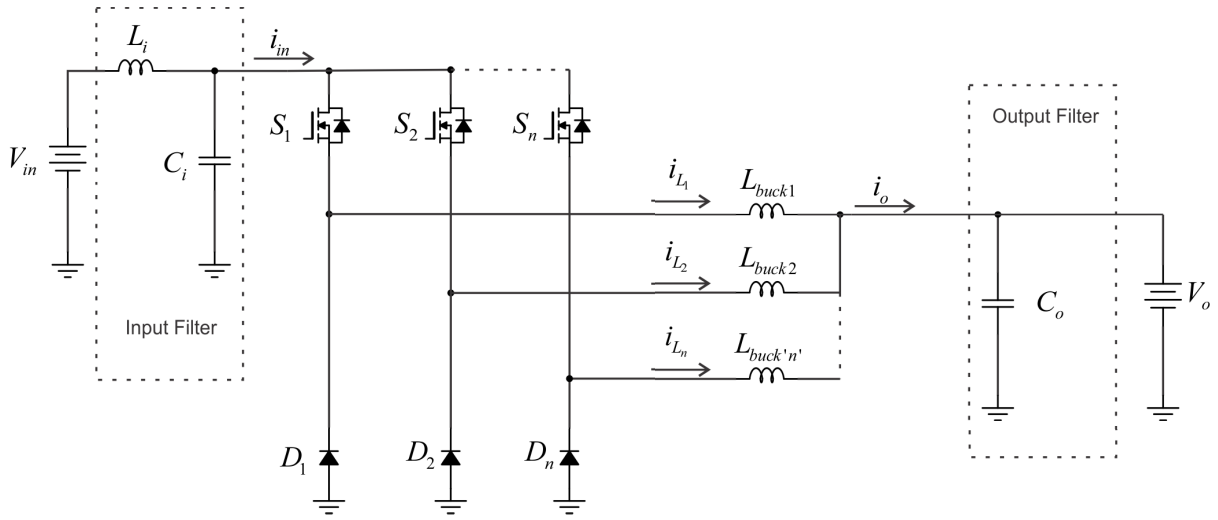
Source: Own Elaborated

As known, to size filters with passive elements, the volume of the filter will depend on the energy processed on it and the frequency to be filtered. Looking at Figures 5.11 and 5.12, it is possible to conclude that the total waveforms appear on the double of the switching frequency, allowing the volume reduction of the filters.

5.6.2 Interleaved Buck Input Filter

Figure 5.13 presents a schematic of a n level Buck Converter. From equation (5.71), it can be obtained the ripple voltage over the input capacitor. At the complementary operation stage of D_i, the input capacitor must absorb the average input current on the converter subtracted by the sum of the ON switches. In other words, the ON switches, according to the operation point will draw a constant current at interval T_i. So the capacitor current will "see" only the current of one switch to be filtered.

Figure 5.13 – Interleaved Buck



Source: Own elaborated

From equation (5.71), it can be obtained the ripple voltage over the input capacitor. At the complementary operation stage of D_i, the input capacitor must absorb the average input current on the converter subtracted by the sum of the ON switches. In other words, the ON switches, according to the operation point will draw a constant current at interval T_i. So the capacitor current will "see" only the current of one switch to be filtered.

$$i_{C_i} = C_i \frac{dv_{C_i}}{dt} \tag{5.71}$$

$$i_{C_i} = I_{in} - (n_{on} \cdot I_{L_{buck}}) \tag{5.72}$$

Knowing that the sum of inductor's current is equal to the output current, and the input current is equal to $I_o D$, then:

$$[I_{in} - (n_{on} \cdot I_{L_{buck}})] = C_i \frac{\Delta v_{C_i}}{\Delta t} \tag{5.73}$$

$$[I_{in} - (n_{on} \cdot I_{L_{buck}})] = C_i \frac{\Delta v_{C_i}}{(1 - D_i)\, T_{Si}} \tag{5.74}$$

$$\left[I_o \cdot D - \left(n_{on} \cdot \frac{I_o}{n}\right)\right] = C_i \frac{\Delta v_{C_i}}{(1 - D_i)\, T_{Si}} \tag{5.75}$$

As known:

$$T_{Si} = \frac{T_S}{n} \tag{5.76}$$

Replacing equation (5.76) at equation (5.75) and rearranging terms:

$$\frac{I_o}{n} \cdot \underbrace{\left[n \cdot \left(D - \frac{n_{on}}{n}\right)\right]}_{D_i} \cdot \left(\frac{1 - D_i}{n}\right) \cdot T_S = C_i \cdot \Delta v_{C_i} \tag{5.77}$$

So the expression of ripple voltage at capacitor can be described as:

$$\Delta v_{C_i} = \frac{I_o}{C_i \cdot f_S} \cdot \left[\frac{D_i}{n} \cdot \left(\frac{1 - D_i}{n}\right)\right] \tag{5.78}$$

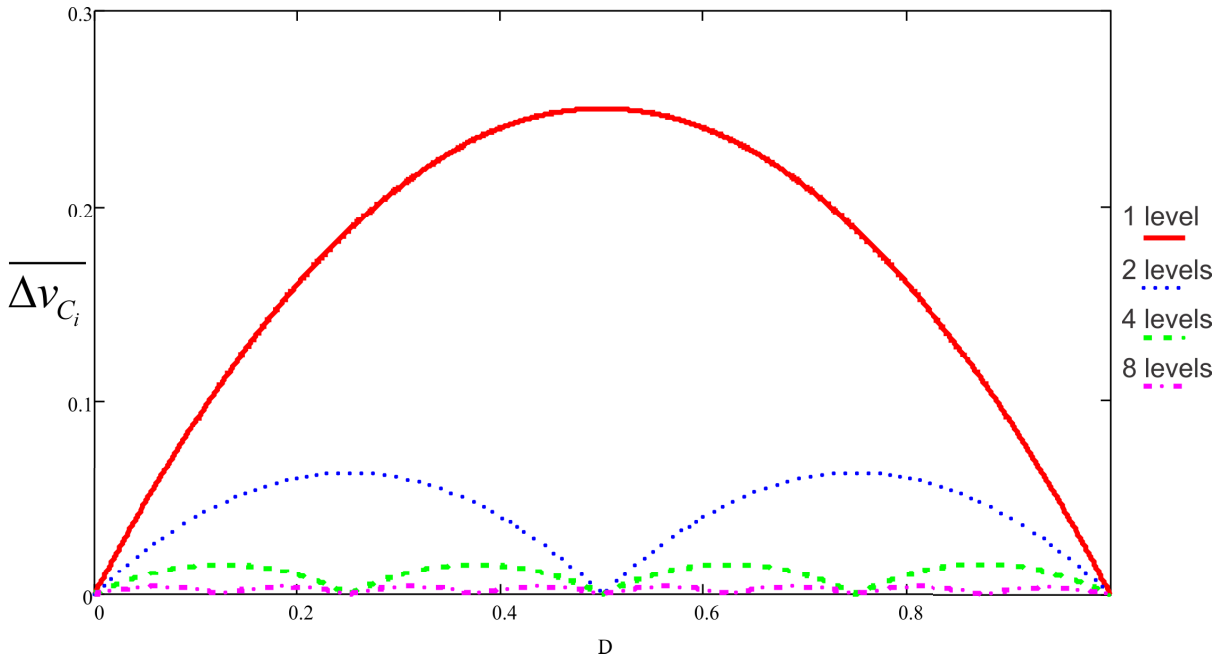
Normalizing equation (5.78):

$$\overline{\Delta v_{C_i}} = \frac{C_i \cdot f_S}{I_o} \cdot \Delta v_{C_i} \tag{5.79}$$

$$\overline{\Delta v_{C_i}} = \left[\frac{D_i}{n} \cdot \left(\frac{1 - D_i}{n}\right)\right] \tag{5.80}$$

Figure 5.14 presents the normalized ripple voltage at the capacitor, depending on the number of interleaved converters and the operating duty cycle.

Figure 5.14 – Ripple voltage at input capacitor



Source: Own elaborated

The point of maximum ripple can be found by deriving the equation (5.78) with respect to D_i. Then:

$$\frac{\partial \left[D_i \left(1 - D_i\right)\right]}{\partial D_i} = 0 \rightarrow D_i = \frac{1}{2} \tag{5.81}$$

In this way, the following equation gives the maximum ripple voltage:

$$\Delta v_{C_i} = \frac{I_o}{C_i \cdot f_S} \cdot \frac{1}{4 \cdot n^2} \tag{5.82}$$

Then, to size the input capacitor in respect to the ripple voltage:

$$C_i = \frac{I_o}{4 \cdot \Delta v_{C_i} \cdot f_S \cdot n^2} \tag{5.83}$$

The filter inductor can be sized from:

$$v_{L_i} = L_i \cdot \frac{di_{L_i}}{dt} \tag{5.84}$$

$$L_i \cdot \Delta i_{L_i} = \int v_{L_i}(t) \cdot dt \tag{5.85}$$

Similarly to the calculation for a single converter, the voltage applied to the inductor will be the ripple voltage at the input capacitor. Then:

$$\int_{D_i T_{Si}}^{D_i T_{Si} + \frac{T_{Si}}{2}} \Delta v_{C_i}(t) \cdot dt = \underbrace{\frac{T_{Si}}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_i}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{5.86}$$

Therefore:

$$\Delta i_{L_i} = \frac{\Delta v_{C_i}}{8 \cdot L_i \cdot f_S \cdot n} \tag{5.87}$$

Also:

$$\Delta i_{L_i} = \frac{I_o \cdot D_i \cdot (1 - D_i)}{8 \cdot L_i \cdot C_i \cdot f_S^2 \cdot n^3} \tag{5.88}$$

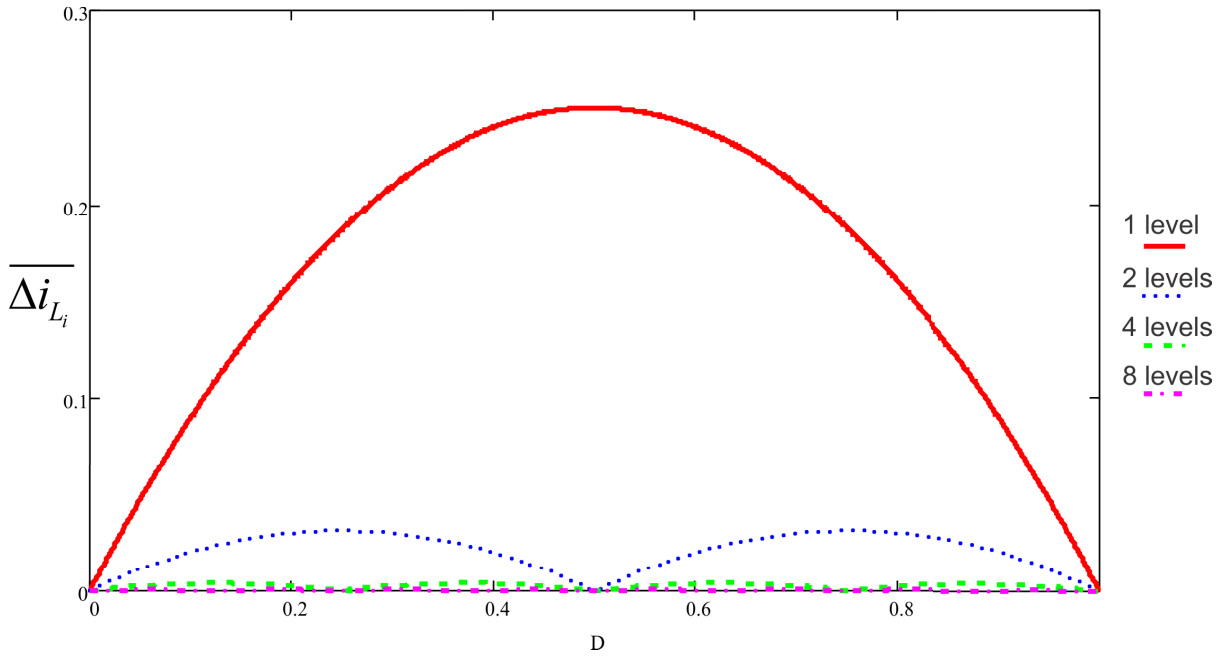
Normalizing equation (5.88):

$$\overline{\Delta i_{L_i}} = \frac{8 \cdot L_i \cdot C_i \cdot f_S^2}{I_o} \cdot \Delta i_{L_i} \tag{5.89}$$

$$\overline{\Delta i_{L_i}} = \frac{D_i \cdot (1 - D_i)}{n^3} \tag{5.90}$$

From equation (5.90), it can be obtained the Figure 5.15, which shows the input ripple current according to the duty cycle and the number of interleaved Buck converters.

Figure 5.15 – Ripple current on the input inductor



Source: Own elaborated

The maximum ripple can be found by the derivative of (5.88) in respect to D_i.

$$\frac{\partial \left[D_i \left(1 - D_i\right)\right]}{\partial D_i} = 0 \rightarrow D_i = \frac{1}{2} \tag{5.91}$$

Therefore:

$$\Delta i_{L_i} = \frac{I_o}{8 \cdot L_i \cdot C_i \cdot {f_S}^2} \cdot \frac{1}{n^3} \left[\left(\frac{1}{2}\right) \cdot \left(1 - \frac{1}{2}\right)\right] \tag{5.92}$$

$$\Delta i_{L_i} = \frac{I_o}{32 \cdot L_i \cdot C_i \cdot {f_S}^2 \cdot n^3} \tag{5.93}$$

Thus the input inductor can be sized as:

$$L_i = \frac{I_o}{32 \cdot \Delta i_{L_i} \cdot C_i \cdot {f_S}^2 \cdot n^3} \tag{5.94}$$

5.6.3 Interleaved Buck Output Filter

The output capacitor must keep the ripple current at the output of the interleaved converters. In the first subinterval $D_i T_{Si}$, the waveform of output current is the sum

of the currents on the active switches and active diodes. Hence the output current is defined by:

$$\left[\underbrace{\left(\frac{V_{in}-V_o}{L_{buck}}\right)(n_{on}+1)}_{on\ switches}-\underbrace{\frac{V_o}{L_{buck}}(n_{off})}_{on\ diodes}\right]\cdot D_i\cdot T_{Si}{=}\Delta i_o \tag{5.95}$$

Replacing (A.3) and (5.3) at (5.95) and rearranging the formula:

$$\Delta i_o=\frac{1}{n}\cdot\left(D_i-D_i^2\right)\cdot\frac{V_{in}}{L_{buck}\cdot f_S} \tag{5.96}$$

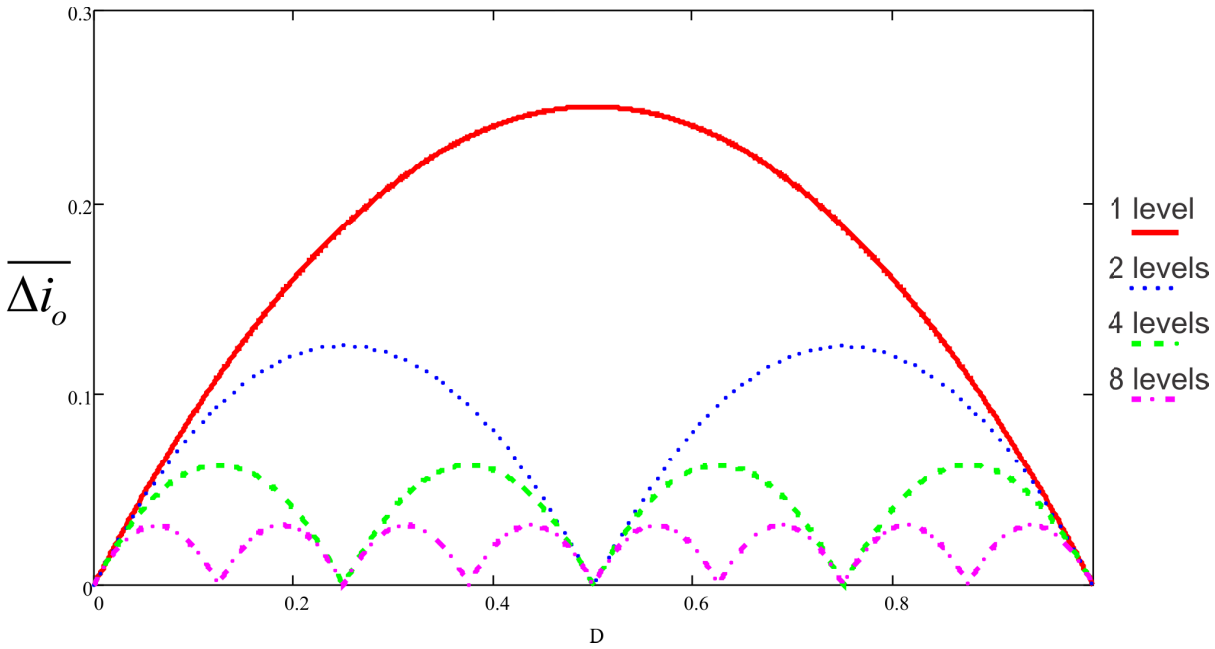
Normalizing equation (5.96):

$$\overline{\Delta i_o}=\frac{L_{buck}\cdot f}{V_{inS}}\cdot\Delta i_o \tag{5.97}$$

$$\overline{\Delta i_o}=\frac{1}{n}\cdot\left(D_i-D_i^2\right) \tag{5.98}$$

From equation (5.98) is obtained the graph of output ripple current, according to the interleaved converters and the operating duty cycle presented in Figure 5.16.

Figure 5.16 – Ripple current at output of interleaved converters



Source: Own elaborated

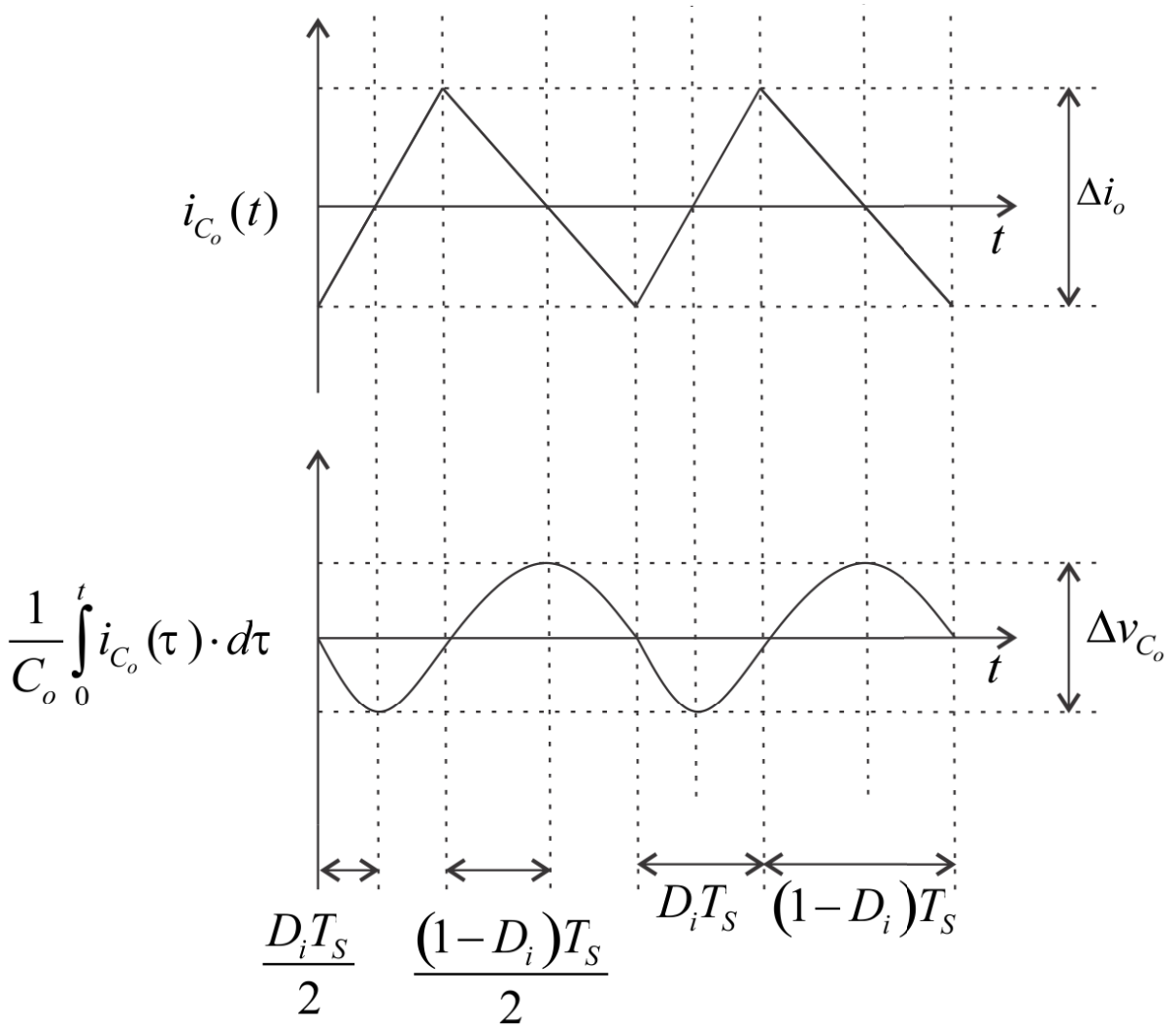
Considering that the capacitor will keep the ripple current, it can be calculated the ripple voltage:

$$i_{C_o}=C_o\frac{dv_{C_o}}{dt} \tag{5.99}$$

$$v_{C_o}(t) = V_o + \frac{1}{C_o}\int_0^t i_{C_o}(\tau)\cdot d\tau \tag{5.100}$$

Thus, it is possible to plot the graph of ripple voltage on the output capacitor, according to Figure 5.17.

Figure 5.17 – Ripple voltage at output capacitor



Source: Own elaborated

The ripple voltage on the output capacitor can be obtained by the area of the triangle calculation formed by the capacitor current, as shown in Figure 5.17.

$$\Delta v_{C_o} = \frac{1}{C_o}\underbrace{\left[\frac{D_i}{2} + \frac{1-D_i}{2}\right]T_{Si}}_{base}\cdot\underbrace{\left[\frac{\Delta i_o}{2}\right]}_{height}\cdot\underbrace{\left[\frac{1}{2}\right]}_{\div 2} \tag{5.101}$$

$$\Delta v_{C_o} = \frac{V_{in}\left(D_i - {D_i}^2\right)}{8\cdot C_o\cdot {f_S}^2\cdot n^2\cdot L_{buck}} \tag{5.102}$$

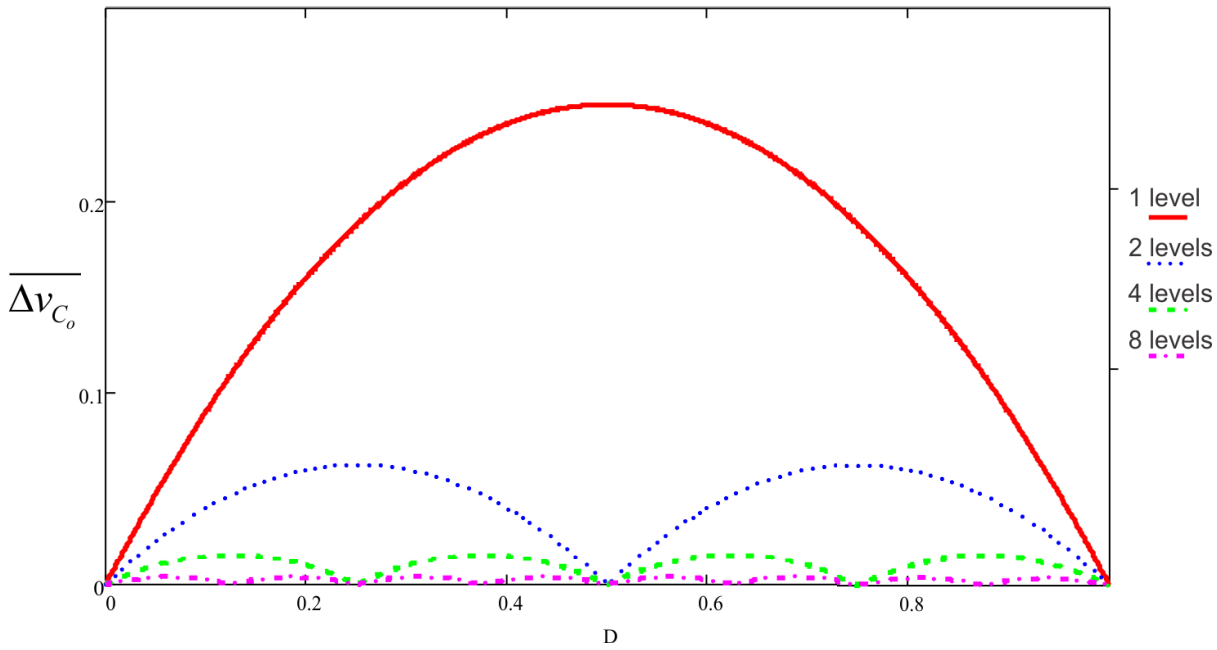
Normalizing equation (5.102):

$$\overline{\Delta v_{C_o}} = \frac{8 \cdot C_o \cdot {f_S}^2 \cdot L_{buck}}{V_{in}} \cdot \Delta v_{C_o} \tag{5.103}$$

$$\overline{\Delta v_{C_o}} = \frac{\left(D_i - {D_i}^2\right)}{n^2} \tag{5.104}$$

From equation 5.102, it is possible to obtain the graph of normalized ripple voltage at capacitor presented in Figure 5.18.

Figure 5.18 – Normalized ripple voltage at output capacitor



Source: Own elaborated

Maximizing equation (5.102) in function of D_i, the capacitor can be calculated as:

$$C_o = \frac{V_{in}}{32 \cdot \Delta v_{C_o} \cdot {f_S}^2 \cdot n^2 \cdot L_{buck}} \tag{5.105}$$

5.7 PARTIAL CONCLUSIONS

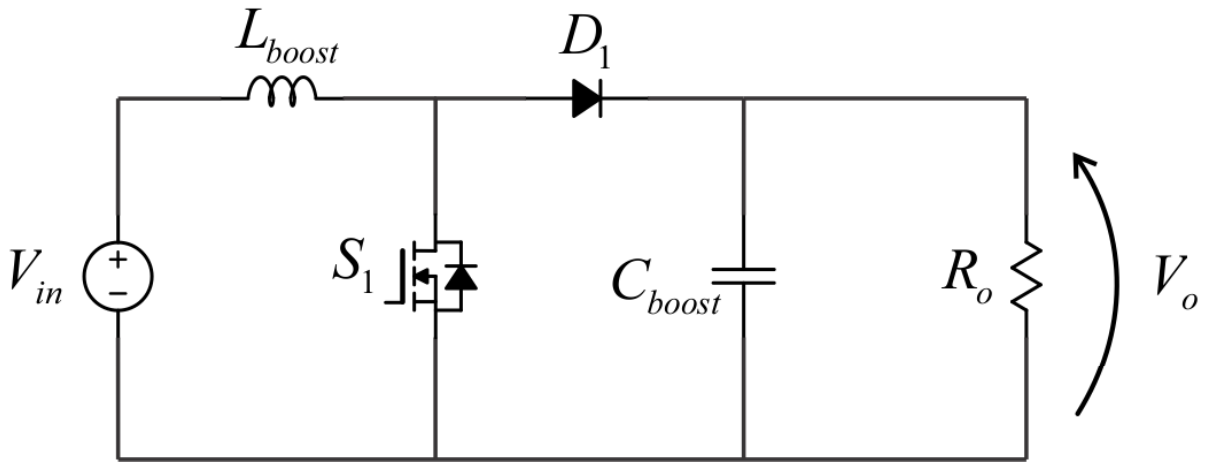
Among the step-down converters, the Buck stands out by the reduced number of semiconductors and its simplicity to modulate. As a consequence, the CCM operation is formed by two topological states. With the addition of filters, the Buck can be used to operate with batteries in the input as the source, and on the output as load.

The converter can be derived NIBB. As well, interleaving modules can reduce filter size. Its combination with the Boost converter allows the utilization of the implemented architecture. Boost characteristics are presented in the next chapter.

6 STUDY OF BOOST CONVERTER IN CONTINUOUS CONDUCTION MODE

The DC Boost converter is characterized by an input power supply, an inductor, a diode, a switch, a capacitor, and an output load. Its topology can be seen in Figure 6.1.

Figure 6.1 – DC Boost topology



Fonte: Own Elaborated

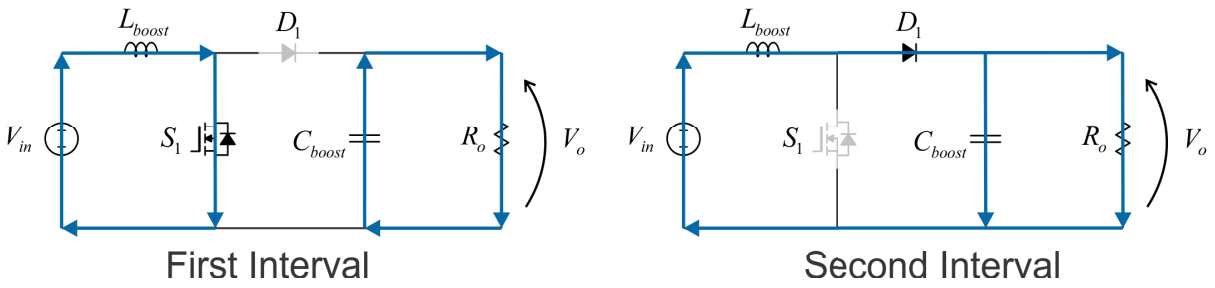
6.1 MODULATION

In the same way of Buck converter, the Boost modulation will be the result of a comparison between a carrier and the modulation signal, for the purpose of defining which duty cycle will be applied to the switch S_1, as presented in Figures 5.2 and 5.3.

6.2 TOPOLOGICAL STATES

In Continuous Conduction Mode (CCM), the converter operates in two different topological states. In the first subinterval, the switch is closed, ramping up the current on the inductor. In the second subinterval, the switch is opened and the diode starts conducting, assuming the inductor current. Those topological states are conferred in Figure 6.2.

Figure 6.2 – Topological States of Boost Converter



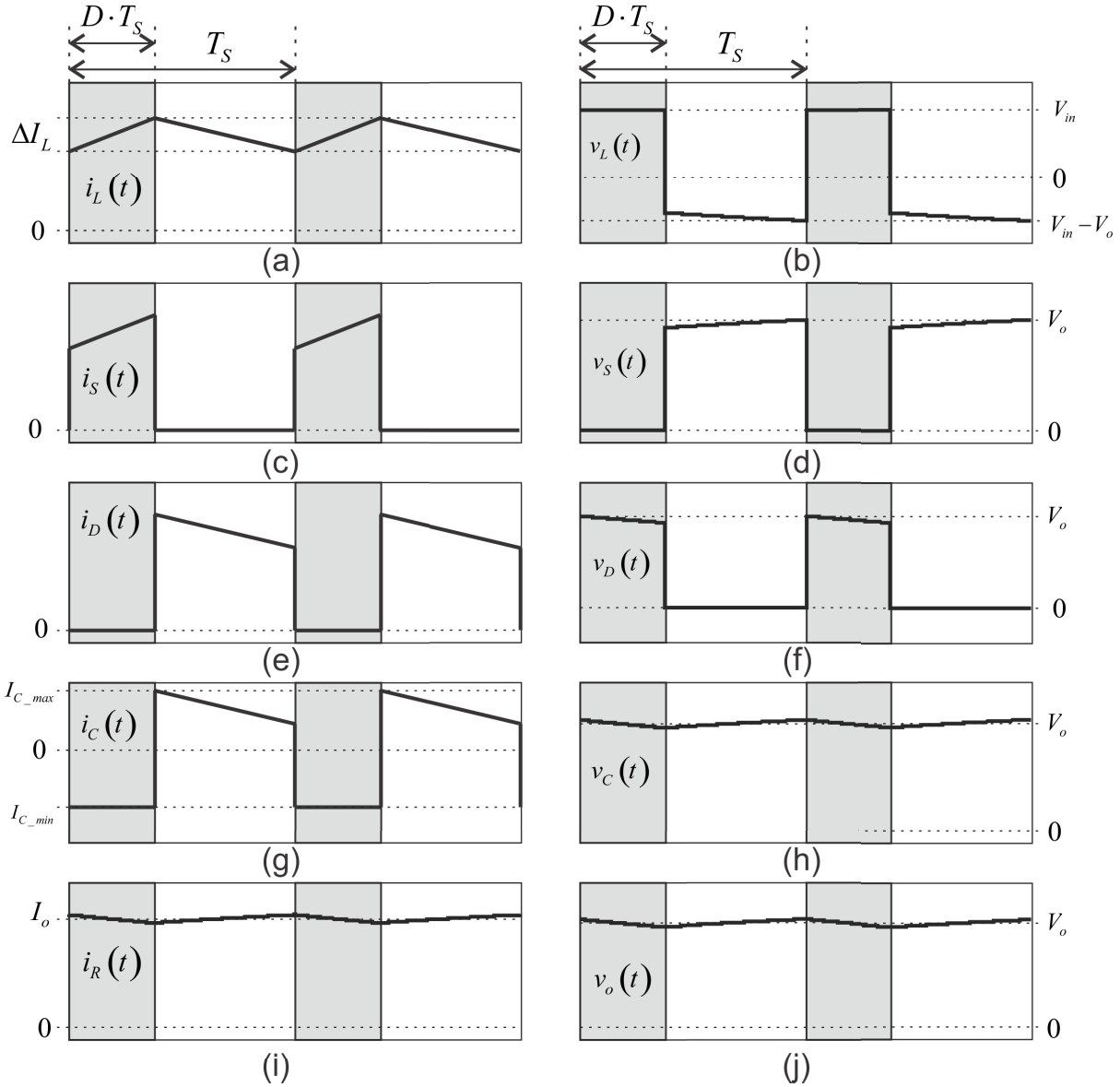
Source: Own Elaborated

6.3 WAVEFORMS

The waveforms of the two topological states mentioned in the past subsection are presented in Figure 6.3:

- current 6.3a and voltage 6.3b on the inductor;
- current 6.3c and voltage 6.3d on the switch;
- current 6.3e and voltage 6.3f on the diode;
- current 6.3g and voltage 6.3h on the capacitor;
- current 6.3i and voltage 6.3j on the output resistor.

Figure 6.3 – Boost CCM Waveforms



Source: Own elaborated

6.4 ALGEBRAIC ANALYSIS

Following the last chapter, the average values of voltage and current will be represented by uppercase letters, while the time-variant values will be in lowercase letters.

6.4.1 Inductor

The average voltage on the inductor can be found by the equation:

$$V_{L_{boost}} = \frac{V_{in} \cdot D \cdot T_S + (V_{in} - V_o) \cdot (1 - D) \cdot T_S}{T_S} \tag{6.1}$$

In steady-state, there is no energy storage on the inductor in a switching interval. Therefore the average voltage is zero. Matching the equation (6.1) to zero, and performing the needed adjustments, it is obtained:

$$V_o = \frac{V_{in}}{1 - D} \tag{6.2}$$

The static gain is given by:

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D} \tag{6.3}$$

To found the ripple current, it is used the basic equation of an inductor:

$$v_{L_{boost}} = L_{boost} \frac{di_{L_{boost}}}{dt} \tag{6.4}$$

As seen in Figure 6.3, in the subinterval between 0 and DT_S, the current goes from its minimum value reaching its peak. Then:

$$\frac{di_{L_{boost}}}{dt} = \frac{\Delta i_{L_{boost}}}{\Delta t} \tag{6.5}$$

Hence:

$$V_{in} = L_{boost} \frac{\Delta i_{L_{boost}}}{D \cdot T_S} \tag{6.6}$$

Using the equation (6.2) in (6.6) and adjusting its variables, it is found the ripple current presented at equation (6.7).

$$\Delta i_{L_{boost}} = \frac{V_o \cdot (1 - D) \cdot D}{L_{boost} \cdot f_S} \tag{6.7}$$

Rearranging equation (6.7), the inductor can be described as:

$$L_{boost} = \frac{V_o \cdot (1 - D) \cdot D}{\Delta i_{L_{boost}} \cdot f_S} \tag{6.8}$$

The average current on the Boost inductor is the average input current.

$$I_{L_{boost}} = I_{in} \tag{6.9}$$

Using the conservation of energy, then:

$$P_{in} = P_o \tag{6.10}$$

$$V_{in} \cdot I_{in} = V_o \cdot I_o \tag{6.11}$$

$$I_{in} = \frac{V_o \cdot I_o}{V_{in}} \tag{6.12}$$

Applying equation (6.3) in (6.12):

$$I_{in} = \frac{I_o}{(1-D)} \tag{6.13}$$

Then:

$$I_{L_{boost}} = \frac{I_o}{(1-D)} \tag{6.14}$$

6.4.2 Capacitor Boost

To provide a continuous voltage on the output, the capacitor of the Boost converter must filter the output current. Capacitor's current is described by:

$$i_{C_{boost}} = C_{boost}\frac{dv_{C_{boost}}}{dt} \tag{6.15}$$

From equation (6.15):

$$i_{C_{boost}} = C_{boost}\frac{\Delta v_{C_{boost}}}{\Delta t} \tag{6.16}$$

In the interval from 0 to DT_S, the diode is blocked. So the capacitor must provide the average current to load, as seen in Figure 6.2.

Thus:

$$I_o = C_{boost}\frac{\Delta v_C}{D \cdot T_S} \tag{6.17}$$

Knowing that:

$$V_o \cdot I_o = V_{in} \cdot I_{in} \tag{6.18}$$

From equations (6.2), (6.17), and (6.18), the voltage ripple is defined as:

$$\Delta v_{C_{boost}} = \frac{I_{in} \cdot D \cdot (1-D)}{C_{boost} \cdot f_S} \tag{6.19}$$

6.4.3 Switch

From Figure 6.3 (c), it is seen that in the interval between 0 to DT_S, the switch current is equal to the inductor current. In the rest of the switching period, it is zeroed. Thus, the average current in the switch is:

$$I_S = \frac{1}{T_S} \int_0^{T_S} i_S(t) \cdot dt \tag{6.20}$$

$$I_S = \frac{1}{T_S} \int_0^{DT_S} i_{L_{boost}}(t) \cdot dt \tag{6.21}$$

The inductor current at the 0 to DT_S interval can be described as:

$$i_{L_{boost}}(t) = I_{L_min} + \frac{V_{in}}{L} \cdot t \tag{6.22}$$

I_{L_min} is defined as the average value subtracted by half of its ripple. As the average inductor current is the same as the average input current, therefore:

$$i_{L_{boost}}(t) = \left(\frac{P_o}{V_{in}} - \frac{V_{in} \cdot D \cdot T_S}{2 \cdot L_{boost}} \right) + \frac{V_{in}}{L_{boost}} \cdot t \tag{6.23}$$

$$i_{L_{boost}}(t) = \left(\frac{P_o}{V_{in}} - \frac{V_{in} \cdot D \cdot T_S}{2 \cdot L_{boost}} \right) + \frac{V_{in}}{L} \cdot t \tag{6.24}$$

So the average switch current is:

$$I_S = \frac{1}{T_S} \int_0^{DT_S} \left[\left(\frac{P_o}{V_{in}} - \frac{V_{in} \cdot D \cdot T_S}{2 \cdot L_{boost}} \right) + \frac{V_{in}}{L} \cdot t \right] \cdot dt \tag{6.25}$$

$$I_s = \frac{P_o \cdot D}{V_{in}} \tag{6.26}$$

Applying equation (6.3) in (6.26):

$$I_s = \frac{P_o \cdot D}{V_o \cdot (1 - D)} \tag{6.27}$$

Hence:

$$I_s = \frac{I_o \cdot D}{(1 - D)} \tag{6.28}$$

The RMS current is calculated from:

$$I_{S_ef} = \sqrt{\int_0^{T_S} \frac{1}{T_S} [i_S(t)]^2 \cdot dt} \tag{6.29}$$

$$I_{S_ef} = \sqrt{\int_0^{DT_S} \frac{1}{T_S}[i_{L_{boost}}(t)]^2 \cdot dt} \tag{6.30}$$

Applying equation (6.23) in (6.30):

$$I_{S_ef} = \sqrt{\int_0^{DT_S} \frac{1}{T_S}\left[\left(\frac{P_o}{V_{in}} - \frac{V_{in}\cdot D}{2\cdot L_{boost}}\right) + \frac{V_{in}}{L_{boost}}\cdot t\right]^2 \cdot dt} \tag{6.31}$$

Solving equation (6.31):

$$I_{S_ef} = \sqrt{D\cdot I_{in}^2 + \frac{D^3\cdot T_S^2\cdot V_{in}}{12\cdot {L_{boost}}^2}} \tag{6.32}$$

The maximum voltage applied to the diode is equal to the output voltage, as presented in Figure 6.3 (d). Thus:

$$V_{S_max} = V_o \tag{6.33}$$

6.4.4 Diode

In the second subinterval, the switch is closed and the inductor current will flow through the diode, as seen in Figure 6.3 (e). The average current can be calculated as:

$$I_D = \frac{1}{T_S}\int_0^{T_S} i_D(t)\cdot dt \tag{6.34}$$

$$I_D = \frac{1}{T_S}\int_{DT_S}^{T_S} i_{L_{boost}}(t)\cdot dt \tag{6.35}$$

The function that describes the inductor current on the DT_S to T_S is:

$$i_{L_{boost}}(t) = I_{L_\max} + \frac{V_{in}-V_o}{L_{boost}}\cdot(t - D\cdot T_S) \tag{6.36}$$

Knowing that:

$$I_{L_max} = I_{L_{boost}} + \frac{\Delta i_L}{2} \tag{6.37}$$

$$I_{L_max} = I_{L_{boost}} + \frac{V_o\cdot(1-D)\cdot D\cdot T_S}{2\cdot L_{boost}} \tag{6.38}$$

Applying equation (6.38) in (6.36):

$$i_{L_{boost}}(t) = I_{L_{boost}} + \frac{V_o\cdot(1-D)\cdot D\cdot T_S}{2\cdot L_{boost}} - \frac{V_o}{L_{boost}}\cdot(t - D\cdot T_S) \tag{6.39}$$

Applying (6.39) in (6.35):

$$I_D = \frac{1}{T_S} \int_{DT_S}^{T_S} \left[I_{L_{boost}} + \frac{V_o \cdot (1-D) \cdot D \cdot T_S}{2 \cdot L_{boost}} + \frac{V_{in} - V_o}{L_{boost}} \cdot (t - D \cdot T_S) \right] \cdot dt \tag{6.40}$$

Solving equation (6.40):

$$I_D = I_{L_{boost}} \cdot (1-D) \tag{6.41}$$

As the average input current is the same as the average inductor current, so:

$$I_D = I_{in} \cdot (1-D) \tag{6.42}$$

The RMS current can be found from:

$$I_{D_ef} = \sqrt{\int_{DT_S}^{T_S} \frac{1}{T_S} [i_{L_{boost}}(t)]^2 \cdot dt} \tag{6.43}$$

Applying equation (6.39) in (6.43):

$$I_{D_ef} = \sqrt{\int_{DT_S}^{T_S} \frac{1}{T_S} \left[I_{L_{boost}} + \frac{V_{in} \cdot D \cdot T_S}{2 \cdot L_{boost}} + \frac{V_{in} - V_o}{L_{boost}} \cdot (t - D \cdot T_S) \right]^2 \cdot dt} \tag{6.44}$$

Solving equation (6.44), the expression that defines the RMS current on diode is:

$$I_{D_ef} = \sqrt{\frac{\left(\begin{array}{c} D^4 \cdot T_S^2 \cdot V_{in}^2 - 2 \cdot D^3 \cdot T_S^2 \cdot {V_{in}}^2 + \\ + D^2 \cdot {T_S}^2 \cdot V_{in}^2 + 12 \cdot I_o^2 \cdot {L_{boost}}^2 \end{array} \right)}{12 \cdot {L_{boost}}^2 \cdot (1-D)}} \tag{6.45}$$

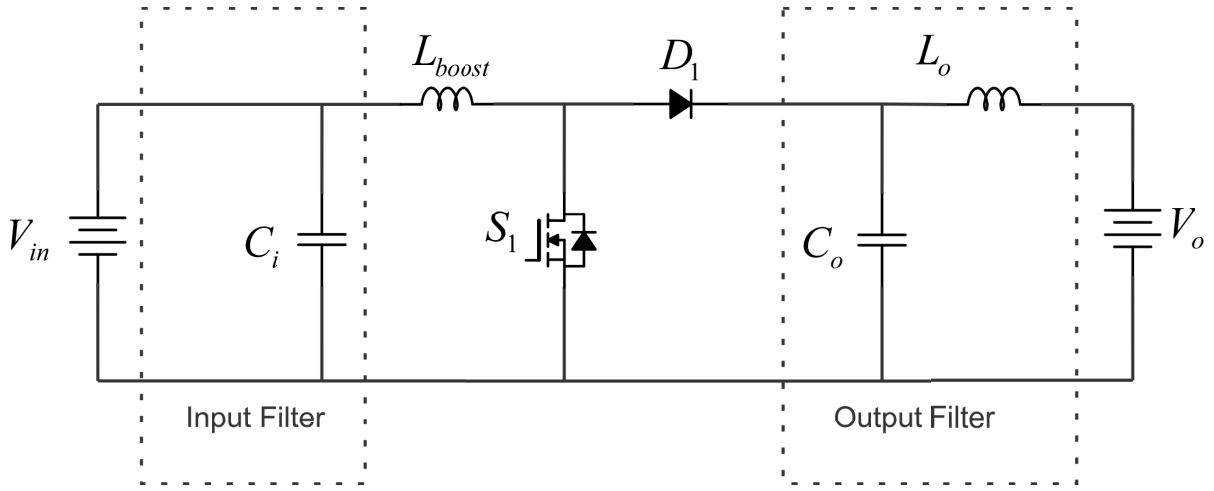
When the diode is blocked, the maximum reverse voltage applied is the output voltage, as shown in Figure 6.3 (f). Hence:

$$V_{D_max} = V_o \tag{6.46}$$

6.5 CONVERTER OPERATION WITH BATTERIES

Likewise the Non-Inverting Buck-Boost, it should be avoided components of high-frequency currents in the batteries. Therefore it is mandatory the addition of input and output filters, as presented in Figure 6.4.

Figure 6.4 – Boost Converter with Batteries



Source: Own Elaborated

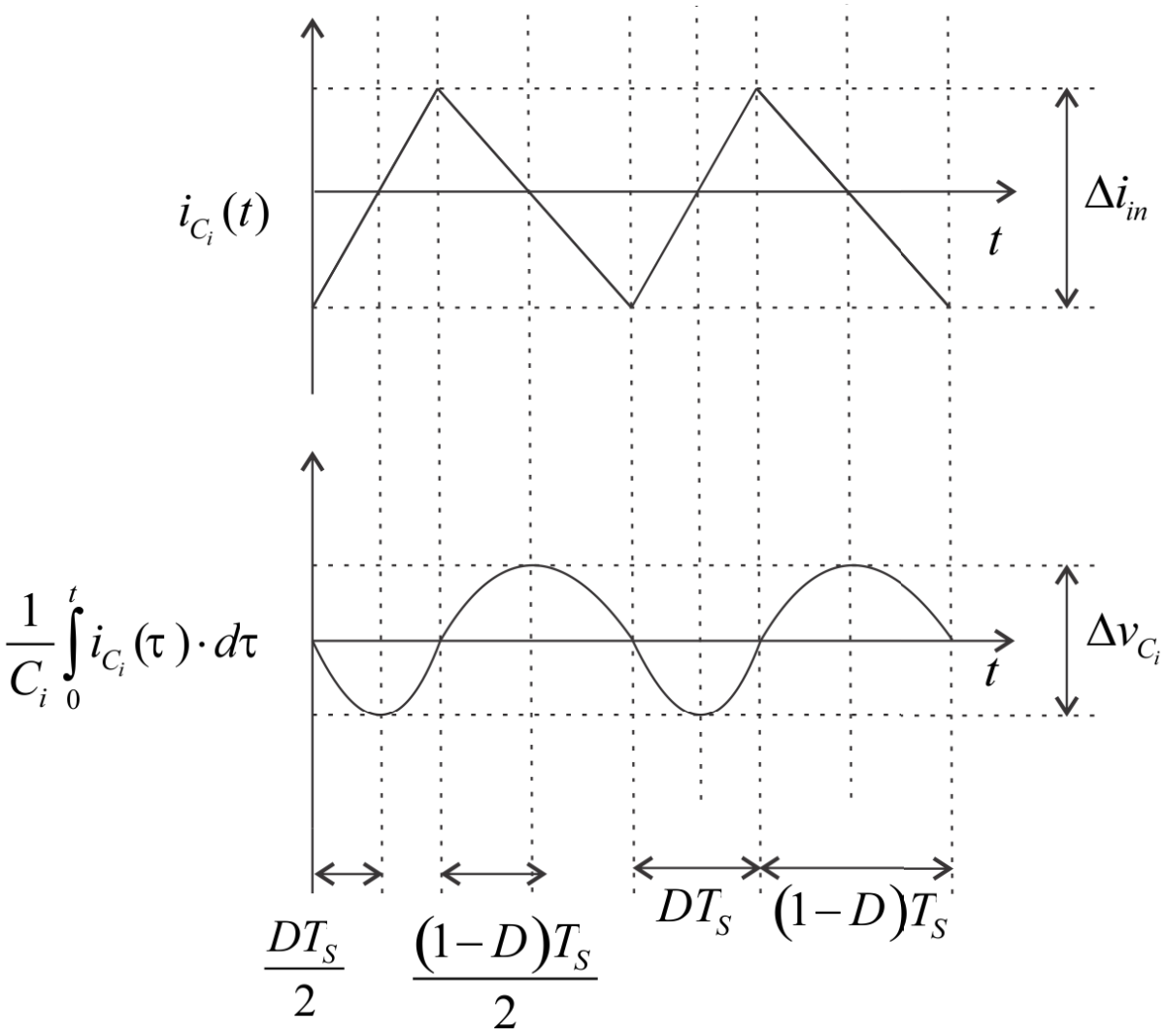
6.5.1 Input filter

The input current of the converter is equal to the inductor current. As a consequence, the input capacitor must keep AC components of that current. To achieve this condition, the L_i impedance must be greater than C_i impedance on the switching frequency. The input current can be described as:

$$i_{C_i} = C_i \frac{dv_{C_i}}{dt} \tag{6.47}$$

Figure 6.5 shows current and voltage ripple on capacitor in a switching interval.

Figure 6.5 – Input capacitor current



Source: Own elaborated

Therefore the ripple voltage can be described as:

$$\Delta v_{C_i} = \frac{1}{C_i} \int_{\frac{DT_S}{2}}^{DT_S+\left[\frac{(1-D)T_S}{2}\right]} i_{C_i}(\tau)\, d\tau \tag{6.48}$$

The integration result is equal to the triangle area over the abscissa axis. It can be calculated as:

$$\Delta v_{C_i} = \frac{1}{C_i} \cdot \left(\underbrace{\frac{T_S}{2}}_{basis} \cdot \underbrace{\frac{\Delta i_{L_{boost}}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \right) \tag{6.49}$$

Replacing (6.7) in equation (6.49), it was obtained the following expression of input capacitor ripple voltage:

$$\Delta v_{C_i} = \frac{V_o \cdot (1-D) \cdot D}{8 \cdot C_i \cdot L_{boost} \cdot f_S^2} \tag{6.50}$$

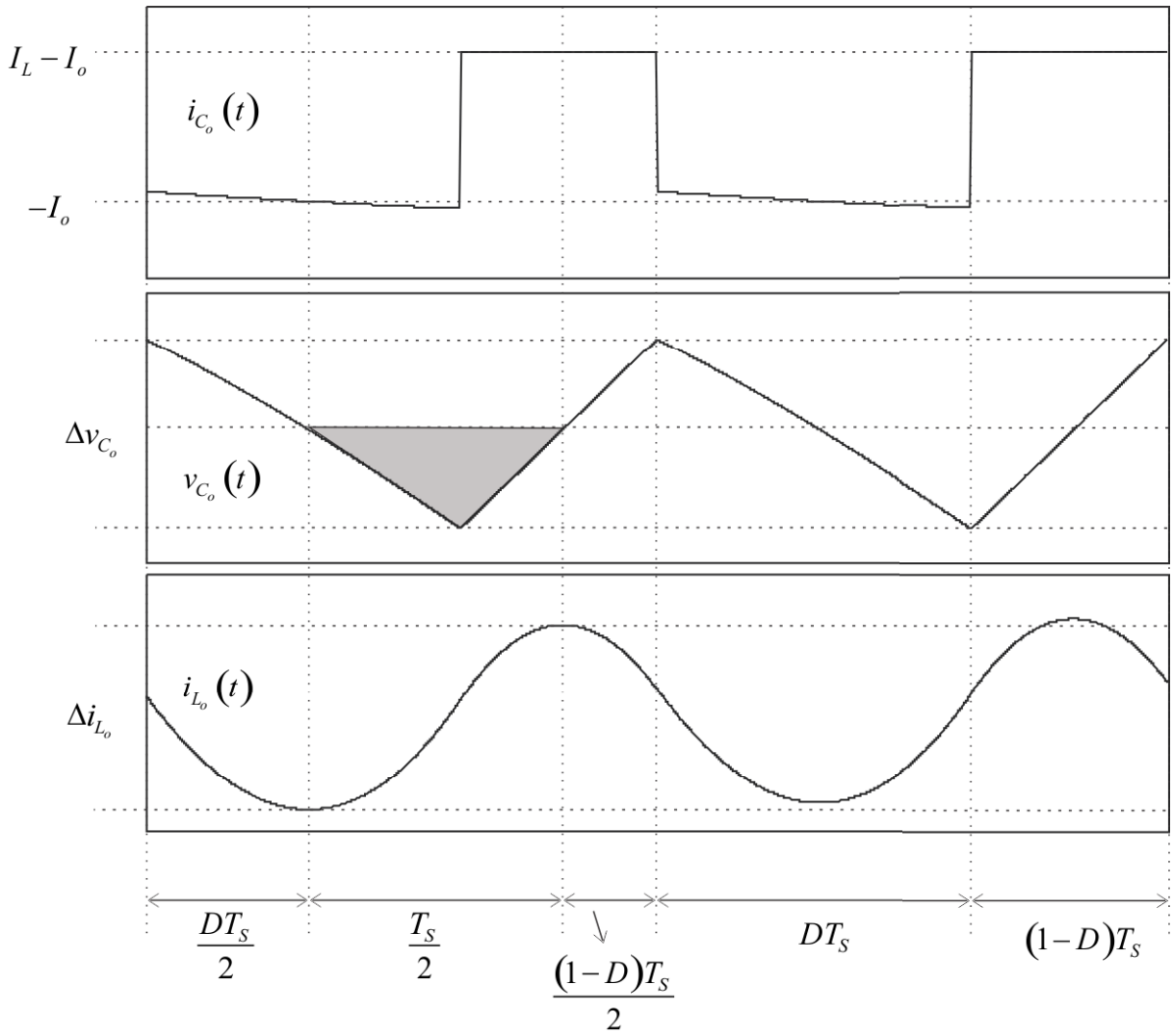
6.5.2 Output filter

Similarly, the output capacitor must absorb the output ripple current. To reach that, the capacitor impedance must be lower than the inductor on the switching frequency.

Capacitor ripple voltage can be defined by equation (6.19).

Figure 6.6 presents the waveforms of current on the output capacitor of Boost converter, output voltage, and current on the filter inductor, respectively.

Figure 6.6 – Waveforms of output filter



Source: Own elaborated

$$\Delta v_{C_o} = \frac{I_{in} \cdot D \cdot (1-D)}{C_o \cdot f_S} \tag{6.51}$$

$$C_o = \frac{I_{in}}{4 \cdot \Delta v_{C_o} \cdot f_S} \tag{6.52}$$

To calculate the output ripple current on filter inductor, it is given:

$$v_{L_o} = L_o \frac{di_{L_o}}{dt} \tag{6.53}$$

According Figure 6.6, the inductor ripple current goes from its minimum value at $\frac{DT_S}{2}$ until its peak on $\frac{DT_S}{2} + \frac{T_S}{2}$. Thus, the ripple can be defined as:

$$\int_{\frac{DT_S}{2}}^{\frac{DT_S}{2}+\frac{T_S}{2}} v_{C_o}(t) \cdot dt = L_o \cdot \Delta i_{L_o} \tag{6.54}$$

The integration result is the calculation of the triangle area, highlighted in Figure 6.6. Thus:

$$\underbrace{\frac{T_S}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_o}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} = L_o \cdot \Delta i_{L_o} \tag{6.55}$$

Hence:

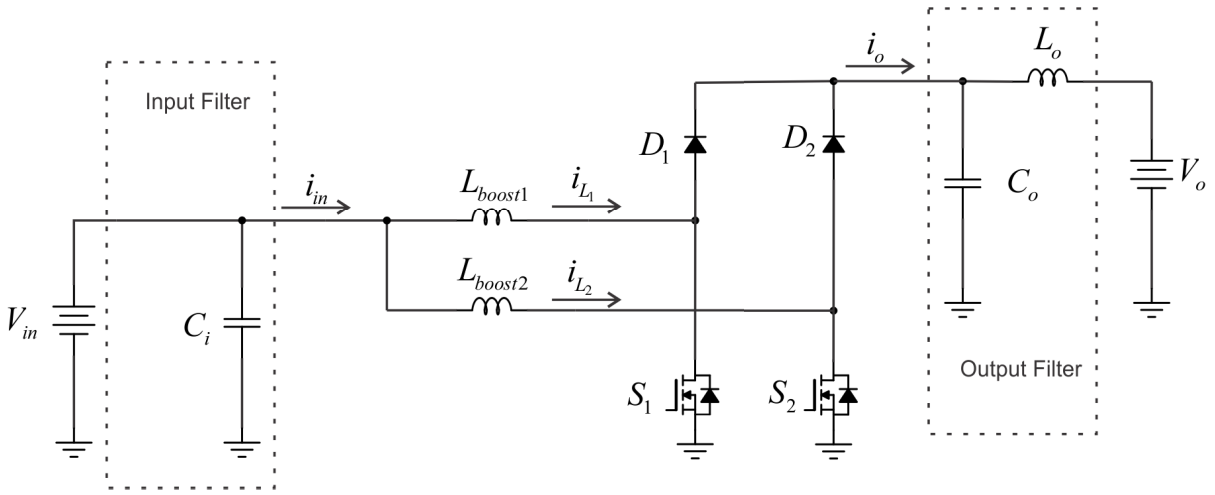
$$\Delta i_{L_o} = \frac{\Delta v_{C_o}}{8 \cdot L_o \cdot f_S} \tag{6.56}$$

$$\Delta i_{L_o} = \frac{I_{in} \cdot D \cdot (1-D)}{8 \cdot C_o \cdot L_o \cdot f_S^2} \tag{6.57}$$

6.6 INTERLEAVING OPERATION

A two-level interleaved Boost converter is presented in Figure 6.7. The phase shift on the carrier signals brings into two possible scenarios considered: at the time greater or smaller than its phase shift. This is presented in Figure 6.8.

Figure 6.7 – Two level boost topology



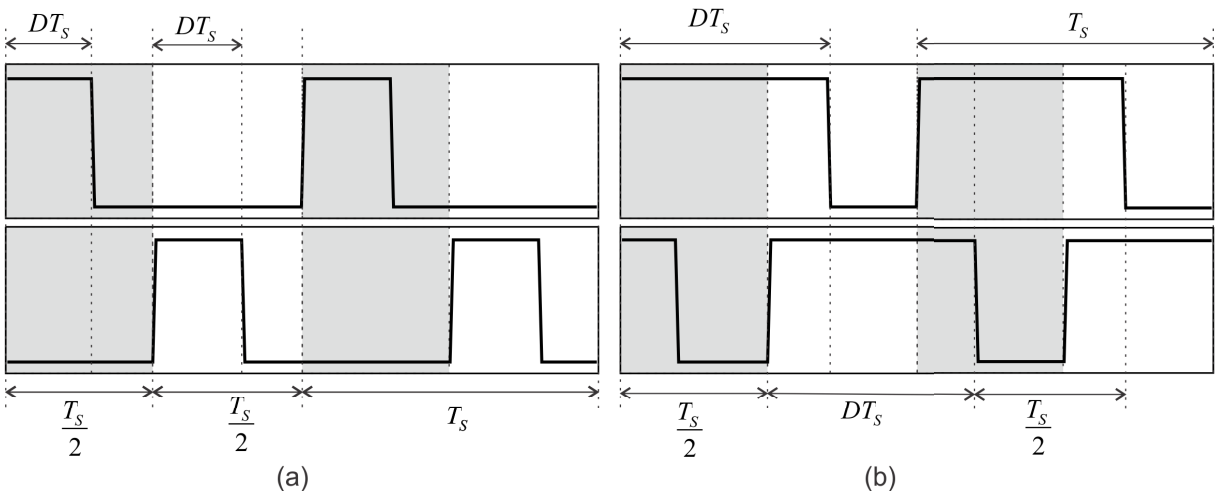
Source: Own elaborated

Given a phase shift of:

$$\theta = \frac{360}{2} = 180 \tag{6.58}$$

$$t_\theta = \frac{T_S}{2} \tag{6.59}$$

Figure 6.8 – Two level boost operating mode



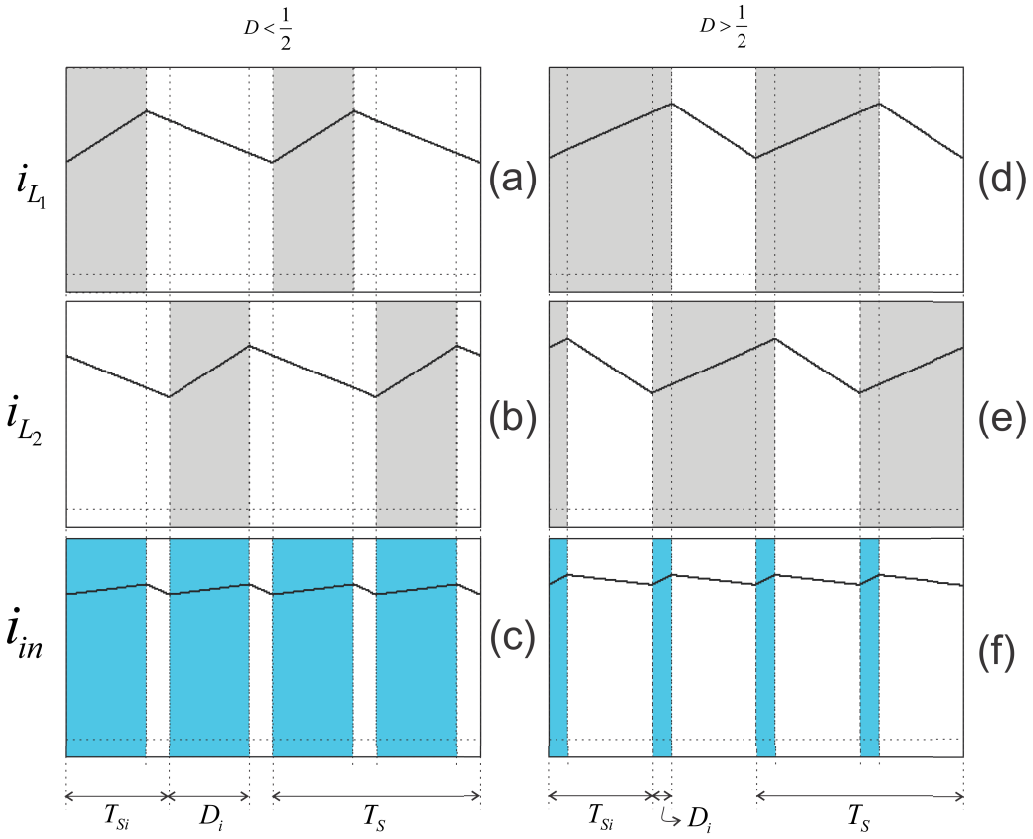
Source: Own elaborated

6.6.1 Changes in the Input and Output Current

Interleaving operation allows the reduction of ripple current, compared to a single converter of the same rated power. Figure 6.9 presents the waveforms of inductor

currents. The resulting input current on the interleaved Boost is the sum of each inductor current.

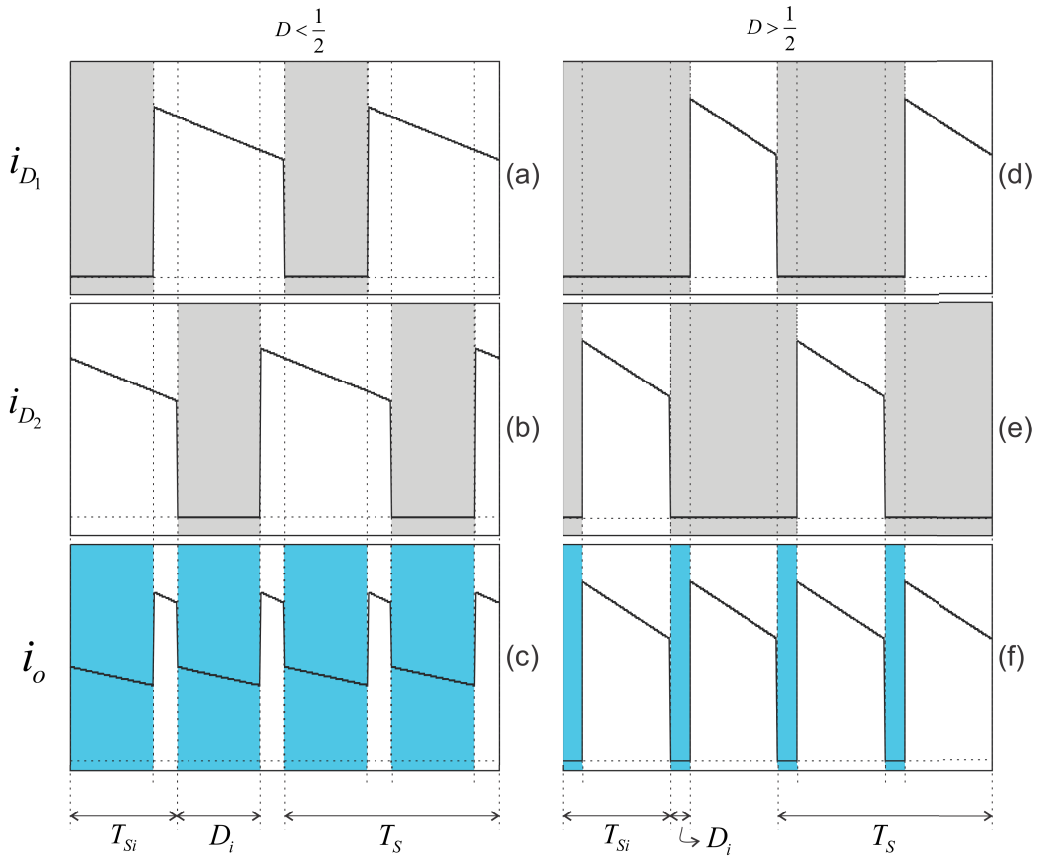
Figure 6.9 – Input current and inductor currents



Source: Own elaborated

Figure 6.10 shows each diode current and its sum, the total output current.

Figure 6.10 – Diodes current and output current

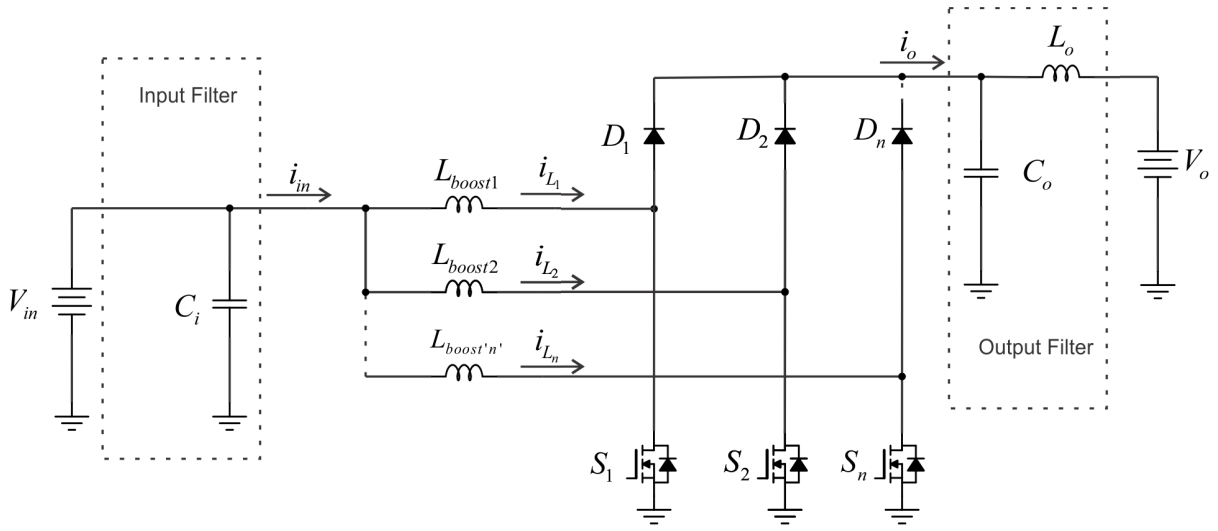


Source: Own elaborated

It is easily noted that the currents on the filter will be reduced using the phase shift technique.

New equations must be defined for the ripple voltage and current calculation on the interleaved converter, using values presented in Appendix A. Thus, it is possible to find those ripples for a "n" level, converter shown in Figure 6.11.

Figure 6.11 – N-level Boost



Source: Own elaborated

6.6.2 Interleaved Boost Input Filter

The ripple voltage can be found from:

$$\Delta i_{in} = \left[\frac{V_{in}}{L_{boost}} \cdot (n_{on}+1) + \frac{V_{in}-V_o}{L_{boost}} \cdot n_{off}\right] \cdot D_i \cdot T_{Si} \tag{6.60}$$

Applying (6.3) in equation (6.60), and adjusting the terms:

$$\Delta i_{in} = \frac{V_o \cdot D_i}{L_{boost} \cdot f_S \cdot n} \cdot [(1-D) \cdot (n_{on}+1) - D \cdot n_{off}] \tag{6.61}$$

Replacing (A.3) in (6.61):

$$\Delta i_{in} = \frac{V_o \cdot D_i}{L_{boost} \cdot f_S \cdot n} \cdot [(1-D) \cdot (n_{on}+1) - D \cdot (n - n_{on} - 1)] \tag{6.62}$$

$$\Delta i_{in} = \frac{V_o \cdot D_i}{L_{boost} \cdot f_S \cdot n} \cdot \left[1 - \underbrace{(-n_{on} + D \cdot n)}_{D_i}\right] \tag{6.63}$$

Thus the input ripple current can be described in equation (6.64).

$$\Delta i_{in} = \frac{V_o}{L_{boost} \cdot f_S \cdot n} \cdot D_i \cdot (1-D_i) \tag{6.64}$$

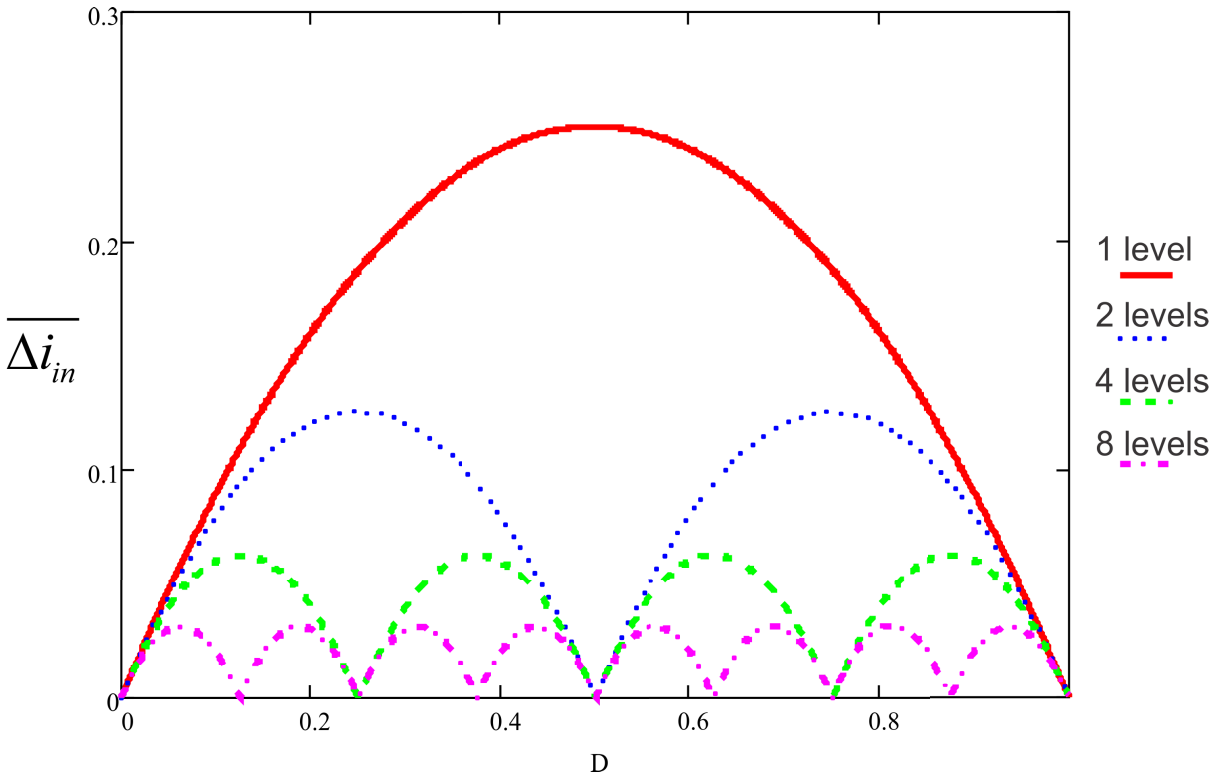
Parameterizing equation (6.64):

$$\overline{\Delta i_{in}} = \frac{L_{boost} \cdot f_S}{V_o} \cdot \Delta i_{in} \tag{6.65}$$

$$\overline{\Delta i_{in}} = \frac{D_i \cdot (1-D_i)}{n} \tag{6.66}$$

Figure 6.12 presents the plot of equation (6.66), according to the duty cycle operation and the number of levels of the converter.

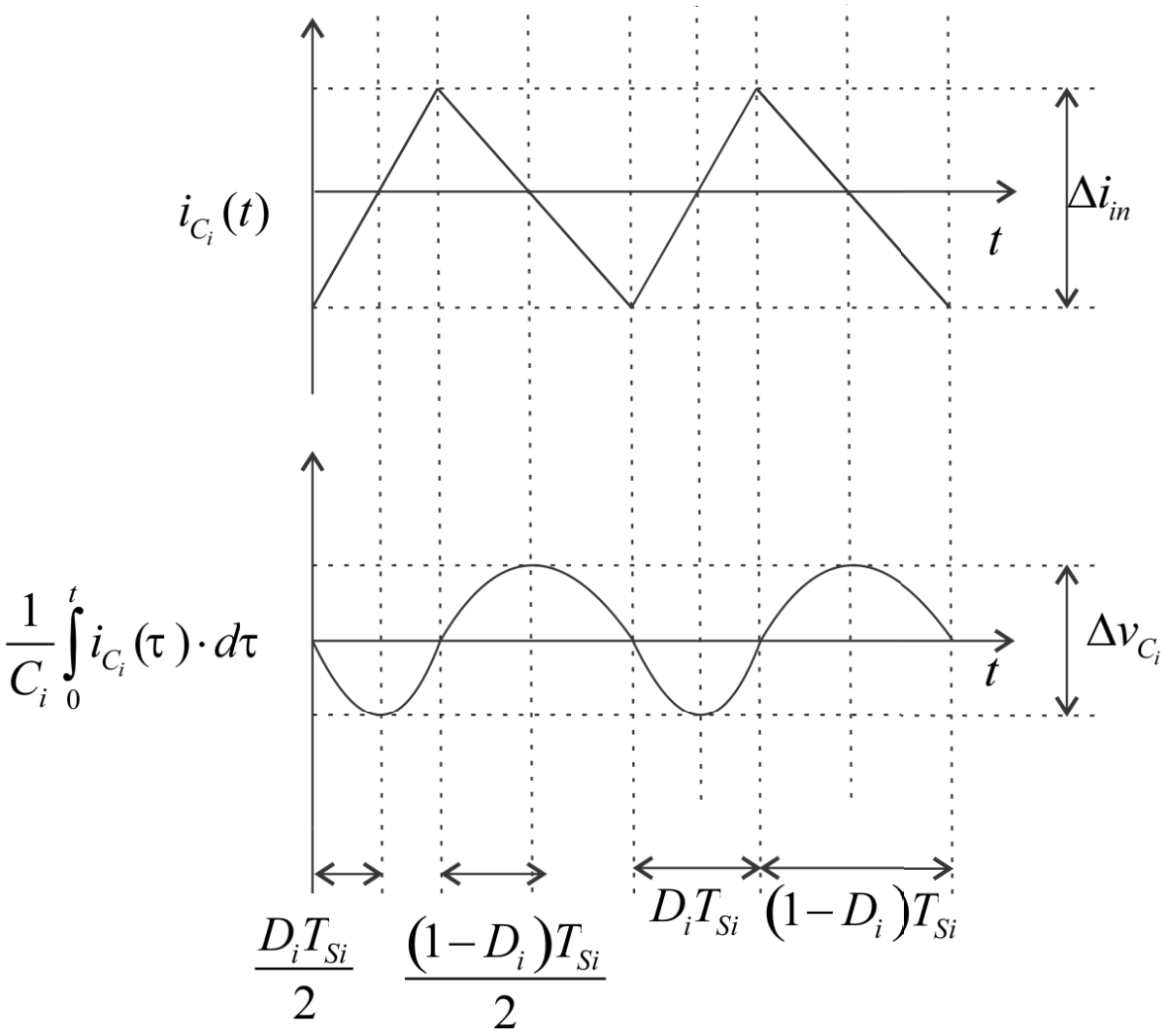
Figure 6.12 – Input Current Ripple



Source: Own elaborated

Considering that capacitor will keep the input AC current, as presented in Figure 6.13, the ripple voltage on the capacitor can be defined as:

Figure 6.13 – Input Capacitor Current



Source: Own elaborated

$$i_{C_i} = C_i \frac{dv_{C_i}}{dt} \tag{6.67}$$

$$C_i \cdot \Delta v_{C_i} = \int_{\frac{D_i T_{Si}}{2}}^{D_i T_{Si} + \frac{(1-D_i)T_{Si}}{2}} i_{C_e}(t)\, dt \tag{6.68}$$

The result of integration is equal to the triangle area over the time axis. Therefore the ripple can be expressed as:

$$C_i \cdot \Delta v_{C_i} = \underbrace{\frac{T_{Si}}{2}}_{basis} \cdot \underbrace{\frac{\Delta i_{in}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} \tag{6.69}$$

Replacing (6.64) in (6.69):

$$\Delta v_{C_i} = \frac{V_o \cdot D_i \cdot (1 - D_i)}{8 \cdot L_{boost} \cdot f_S^2 \cdot n^2 \cdot C_i} \tag{6.70}$$

Normalizing equation (6.70):

$$\overline{\Delta v_{C_i}} = \frac{8 \cdot L_{boost} \cdot f_S^2 \cdot C_i}{V_o} \cdot \Delta v_{C_i} \tag{6.71}$$

$$\overline{\Delta v_{C_i}} = \frac{D_i \cdot (1 - D_i)}{n^2} \tag{6.72}$$

Maximizing equation (6.70) in function of D_i, the capacitor can be sized as:

$$C_i = \frac{V_o}{32 \cdot \Delta v_{C_i} \cdot f_S^2 \cdot n^2 \cdot L_{boost}} \tag{6.73}$$

6.6.3 Interleaved Boost Output Filter

On the interval from $D_i T_S$ to T_S, the capacitor must absorb the AC current of the output inductors. Then:

$$i_{C_o} = C_o \frac{dv_{C_o}}{dt} \tag{6.74}$$

$$I_{L_{boost}} \cdot (n_{off} + 1) - I_o = C_o \frac{\Delta v_{C_o}}{(1 - D_i)\, T_{Si}} \tag{6.75}$$

Once:

$$I_o = n \cdot I_{L_{boost}} \cdot (1 - D) \tag{6.76}$$

Hence:

$$I_{L_{boost}} \cdot (n - n_{on}) - n \cdot I_{L_{boost}} \cdot (1 - D) = C_o \frac{\Delta v_{C_o}}{(1 - D_i)\, T_{Si}} \tag{6.77}$$

$$I_{L_{boost}} \cdot \underbrace{(n \cdot D - n_{on})}_{D_i} = C_o \frac{\Delta v_{C_o}}{(1 - D_i)\, T_{Si}} \tag{6.78}$$

The ripple voltage over the output capacitor can be described as:

$$\Delta v_{C_o} = \frac{I_{L_{boost}} \cdot (1 - D_i) \cdot D_i}{C_o \cdot n \cdot f_S} \tag{6.79}$$

$$\Delta v_{C_o} = \frac{I_{in} \cdot (1 - D_i) \cdot D_i}{C_o \cdot n^2 \cdot f_S} \tag{6.80}$$

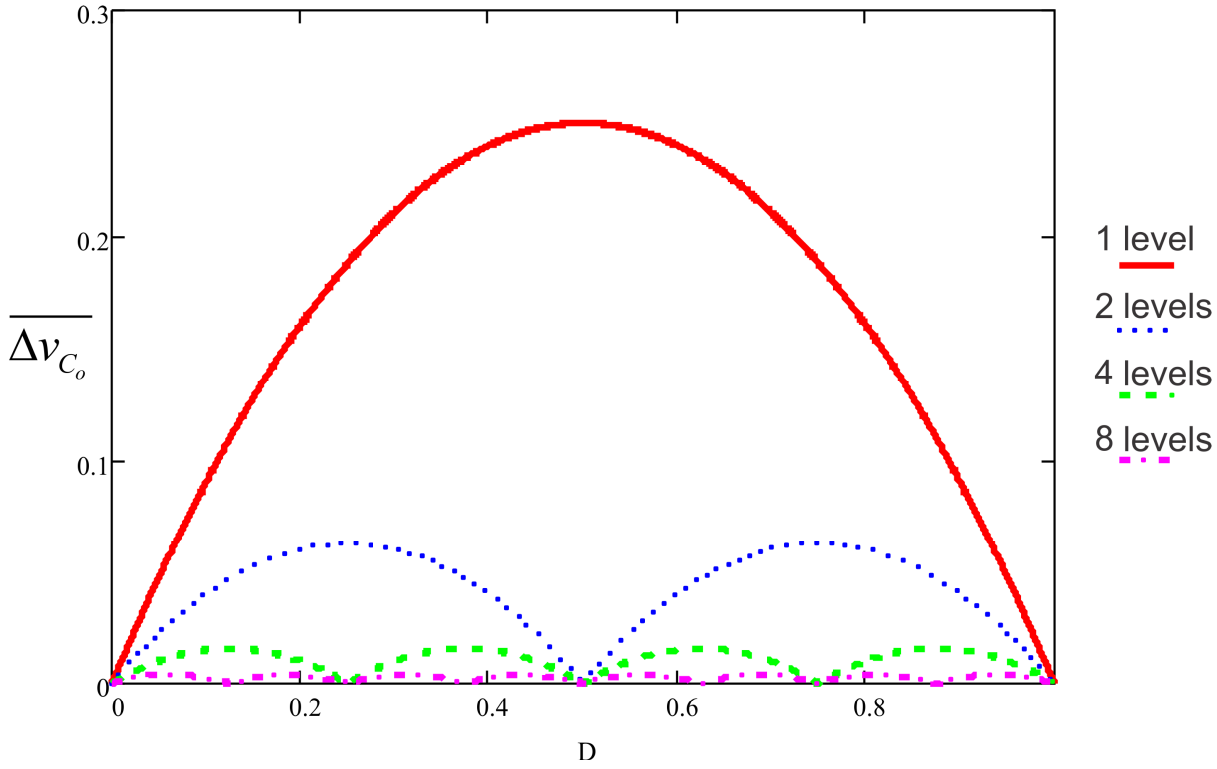
Parameterizing equation (6.80):

$$\overline{\Delta v_{C_o}} = \frac{C_o \cdot f_S}{I_{in}} \cdot \Delta v_{C_o} \tag{6.81}$$

$$\overline{\Delta v_{C_o}} = \frac{(1 - D_i) \cdot D_i}{n^2} \tag{6.82}$$

From equation (6.82), it is obtained the ripple voltage according to the number of interleaved converters and the operating duty cycle, shown in Figure 6.14.

Figure 6.14 – Ripple voltage on output capacitor



Source: Own elaborated

The maximum value of equation (6.80) can be found by:

$$C_o = \frac{I_{in}}{4 \cdot \Delta v_{C_o} \cdot n^2 \cdot f_S} \tag{6.83}$$

The ripple current can be calculated similarly to the filter of a single Boost converter. From Figure 6.6, the ripple is defined as:

$$v_{L_o} = L_o \frac{di_{L_o}}{dt} \tag{6.84}$$

$$L_o \cdot \Delta i_{L_o} = \int_{\frac{D_i T_{Si}}{2}}^{\frac{D_i T_{Si}}{2} + \frac{T_{Si}}{2}} v_{L_o} dt \tag{6.85}$$

$$\underbrace{\frac{T_{Si}}{2}}_{basis} \cdot \underbrace{\frac{\Delta v_{C_o}}{2}}_{height} \cdot \underbrace{\frac{1}{2}}_{\div 2} = L_o \cdot \Delta i_{L_o} \tag{6.86}$$

$$\Delta i_{L_o} = \frac{\Delta v_{C_o}}{8 \cdot L_o \cdot n \cdot f_S} \tag{6.87}$$

Thus the ripple is expressed as:

$$\Delta i_{L_o} = \frac{I_{in} \cdot (1 - D_i) \cdot D_i}{8 \cdot L_o \cdot C_o \cdot n^3 \cdot f_S^2} \tag{6.88}$$

Normatinzing equation (6.88):

$$\overline{\Delta i_{L_o}} = \frac{8 \cdot L_o \cdot C_o \cdot f_S^2}{I_{in}} \cdot \Delta i_{L_o} \tag{6.89}$$

$$\overline{\Delta i_{L_o}} = \frac{(1 - D_i) \cdot D_i}{n^3} \tag{6.90}$$

Maximizing equation (6.88) in function of D_i, the output inductor can be calculated as:

$$L_o = \frac{I_{in}}{32 \cdot \Delta i_{L_o} \cdot C_o \cdot n^3 \cdot f_S^2} \tag{6.91}$$

6.7 PARTIAL CONCLUSIONS

Altogether, the Boost converter allows the transfer between a lower to a higher voltage. Also, the use of the converter in interleaving mode has the same advantages as the Buck converter.

As previously presented, the Buck and Boost converters can be extracted from the Non-Inverting Buck-Boost converter employing a modulation that allows operating the switches independently.

Thus, once the algebraic model of the converter is found operating as a conventional Buck-Boost and as a cascading Buck with a Boost, it is possible to define mathematically the differences for these scenarios.

7 DESIGN OF NON-INVERTING BUCK-BOOST CONVERTER

The previous chapters presented the NIBB converter operating as a Buck-Boost Converter and as an independent Boost and Buck. From there, it is possible to evaluate the advantages of each model. Table 7.1 shows the equations to project the following converters.

Table 7.1 – Converters Comparison

NIBB Operation	**Buck-Boost**	**Buck**	**Boost**
Input Inductor	$L_i = \frac{I_{L_{bb}}}{32 \cdot \Delta i_{L_i} \cdot C_i \cdot f_S^2 \cdot n^2}$	$L_i = \frac{I_o}{32 \cdot \Delta i_{L_i} \cdot C_i \cdot {f_S}^2 \cdot n^3}$	Not Required
Input Capacitor	$C_i = \frac{I_{L_{bb}}}{4 \cdot \Delta v_{C_i} \cdot f_S \cdot n}$	$C_i = \frac{I_o}{4 \cdot \Delta v_{C_i} \cdot f_S \cdot n^2}$	$C_i = \frac{V_o}{32 \cdot \Delta v_{C_i} \cdot f_S^2 \cdot n^2 \cdot L_{boost}}$
Main Inductor	$L_{bb} = \frac{V_{in} \cdot D}{\Delta i_{L_{bb}} \cdot f_S}$	$L_{buck} = \frac{V_{in} \cdot D \cdot (1-D)}{\Delta i_{L_{buck}} \cdot f_S}$	$L_{boost} = \frac{V_o \cdot (1-D) \cdot D}{\Delta i_{L_{boost}} \cdot f_S}$
Output Capacitor	$C_o = \frac{I_{L_{bb}}}{4 \cdot \Delta v_{C_o} \cdot f_S \cdot n}$	$C_o = \frac{V_{in}}{32 \cdot \Delta v_{C_o} \cdot {f_S}^2 \cdot n^2 \cdot L_{buck}}$	$C_o = \frac{I_{in}}{4 \cdot \Delta v_{C_o} \cdot n^2 \cdot f_S}$
Output Inductor	$L_o = \frac{I_{L_{bb}}}{32 \cdot \Delta i_{L_o} \cdot C_o \cdot f_S^2 \cdot n^2}$	Not Required	$L_o = \frac{I_{in}}{32 \cdot \Delta i_{L_o} \cdot C_o \cdot n^3 \cdot f_S^2}$
Average Current on Main Inductor	$I_{L_{bb}} = I_{in} + I_o$	$I_{L_{buck}} = I_o$	$I_{L_{boost}} = \frac{I_o}{(1-D)}$

Source: Own elaborated

From Table 7.1, it is possible to see that for both types of operation the converter will need input and output filters. For Buck mode, the input is pulsed. Therefore, it presents greater ripples in the input capacitor than the Boost. Similarly, the Boost presents pulsed currents in output. Then it has greater ripples on the output for this condition.

Another point that Table 7.1 explicit is that the input filter for a Buck circuit will require lower size passive elements, compared to Buck-Boost. The same occurs with the output Boost filter, compared to Buck-Boost.

Also, it is necessary to analyze the losses in the semiconductors. When operating the switches simultaneously, switching losses will occur in all semiconductors, all the time. However, when operating as independent Buck and Boost, two scenarios will appear:

- Buck mode operation: switch S_2 will not switch, so there are no losses in this semiconductor, and diode D_2 will show only conduction losses;

- Boost mode operation: switch S_1 remains closed, so only conduction losses are noticed, and diode D_1 does not present any type of losses.

Furthermore, for the operation of the switches simultaneously, the current levels on the main inductor will be higher. For example, when operated in Buck mode, to maintain an output current of 30 A, the average current on the main inductor must be 30 A. For the simultaneous switching, to operate as a step-down with 30 A at the output, the current on the main inductor needs to be higher than the output, since this current is pulsed. The elevation of the current on the main inductor causes increased losses on the semiconductors, not only for conduction but also for switching. Either it will also raise the volume of the inductor to avoid core saturation.

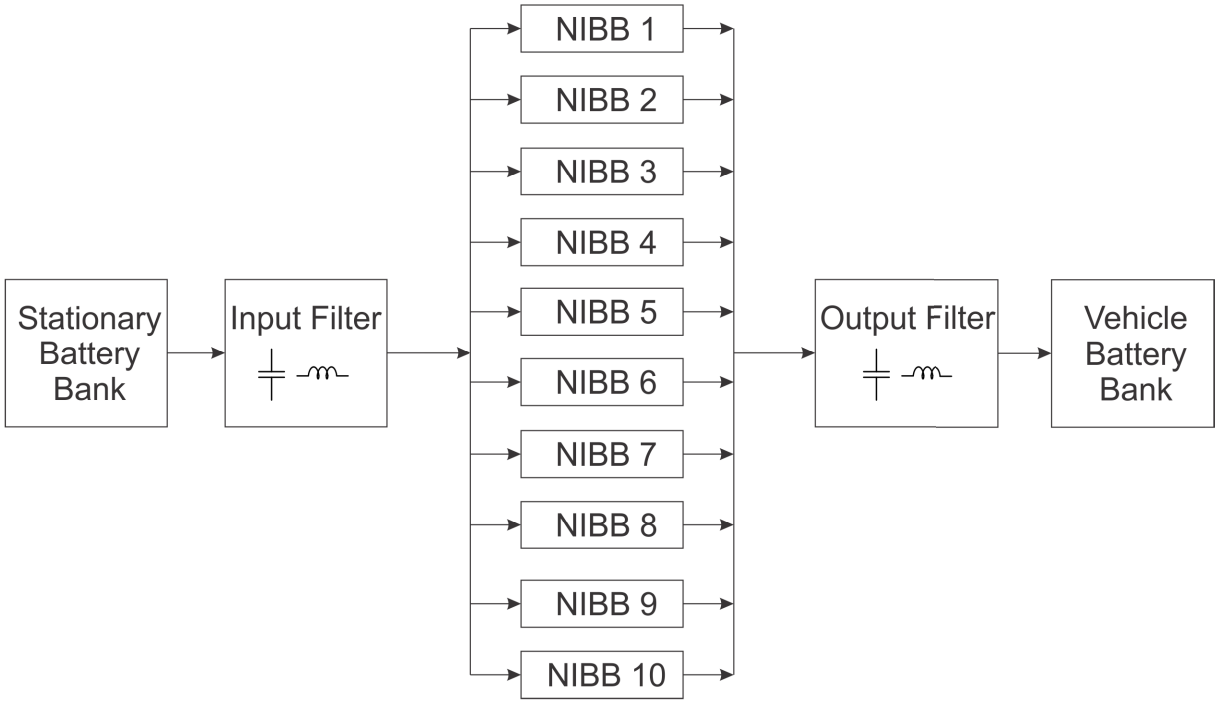
Given the advantages of operating the NIBB converter with different gate signals on the switches, performing as a Buck or Boost circuit, the project was based on that operation.

Once the battery bank capability is known and the converter operation is defined, it is possible to calculate the components of the circuit.

7.1 STRUCTURE

As seen in Chapter 2, the maximum output power of the converter must be around 292.16 kW. Therefore, it was chosen a ten-level NIBB to achieve this total power, as shown in Figure 7.1. In this structure, each converter is 30 kW rated, allowing a total conversion of 300 kW.

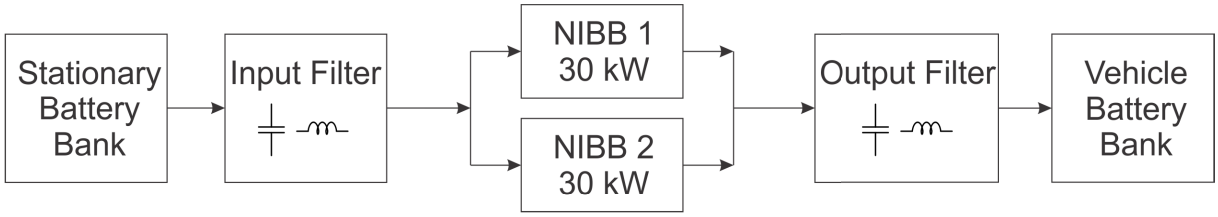
Figure 7.1 – Ten Level NIBB structure



Source: Own Elaborated

However, the implemented converter was made of two converters in parallel, shown in Figure 7.2, validating the structure of the system and the control methods. The project covers the calculation of the passive elements such as inductors and capacitors, the thermal calculations of semiconductors, and its efforts.

Figure 7.2 – Two Level NIBB structure



Source: Own Elaborated

7.2 INPUT PARAMETERS

Following are the parameters used to design each module of the converter:

- Rated power: 30 kW;
- Input voltage: 526 to 730 V;

- Output voltage: 526 to 730 V;
- Ripple current on main inductor: 20 A;
- Ripple voltage at input: 2% of maximum input voltage = 14.6 V;
- Ripple voltage at output: 2% of maximum output voltage = 14.6 V;
- Ripple current at input: 1% of maximum current at main inductor = 0.57 A;
- Ripple current at output: 1% of maximum current at main inductor = 0.57 A;
- Switching frequency: 20 kHz;
- Ambient temperature: 60 °C;

The list of main components used in the project are available in Annex D.

7.3 SEMICONDUCTORS

The first decision is to choose the appropriate semiconductor to use as a switch. The IGBTs can be easily found to adequate in this system due to its high currents capability and high blocking voltages.

To choose the adequate IGBT, it must be considered two main characteristics:

- **The reverse blocking voltage**: in the transition of the IGBT of the ON state to OFF state, there will exist an overvoltage transition, which happens due to the series stray inductances. Therefore, when choosing the correct IGBT, a good practice is to set at least a 50% margin for blocking voltage. This supported blocking voltage is a characteristic of the fabrication process of the semiconductor. When are applied voltages higher than specified, the semiconductor is damaged.
- **Conducting Current**: the conducting current is another parameter that is mandatory to check when choosing IGBT. Besides all datasheets presents a rated current of the semiconductor, to see if is possible the use of it, a thermal calculation must be realized. It implies checking other information on the datasheet, such as energy switching losses; collector-emitter saturation voltage; maximum junction temperature; and thermal resistances. The current capability of a semiconductor is found by how the semiconductor can be cooled up to the junction temperature does not reach its maximum.

The same considerations are valid when choosing a diode.

Once the input and output voltage is imposed by the batteries, the maximum reverse voltage that each semiconductor receives is 730 V. As known, during the switching, a peak voltage appears in the semiconductor. Then, a margin of 50% was considered for this project, resulting in an IGBT and a diode of at least 1100 V rated.

Considering a constant charging current, the maximum output current of each converter is:

$$I_{o_\max} = \frac{30kW}{520V} \tag{7.1}$$

$$I_{o_\max} \approx 57.7A \tag{7.2}$$

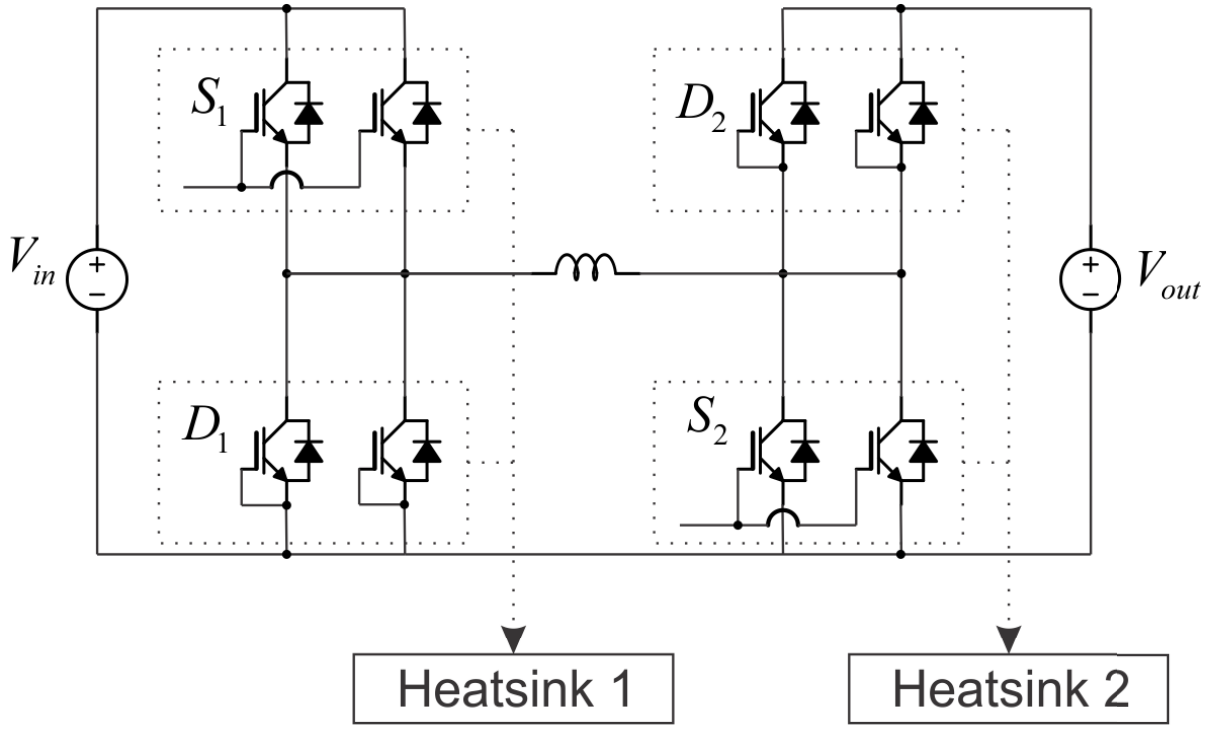
Also, the maximum input current is:

$$I_{in_\max} = \frac{30kW}{520V} \tag{7.3}$$

$$I_{in_\max} \approx 57.7A \tag{7.4}$$

So, the semiconductor used in the project was the IGBT VS-GT100DA120UF from *Vishay*, which is a discrete IGBT with its reverse diode. To increase its capacity, it was used for each component of the topology two semiconductors in parallel, as presented in Figure 7.3. Each commutation cell was placed in a different heatsink. For convenience, it was used the free-wheeling diode of the VS-GT100DA120UF as the diode.

Figure 7.3 – Semiconductors Connection Structure



Source: Own Elaborated

The IGBTs and diodes were chosen once the thermal model meets the project specifications. The ambient temperature considered was 60 °C.

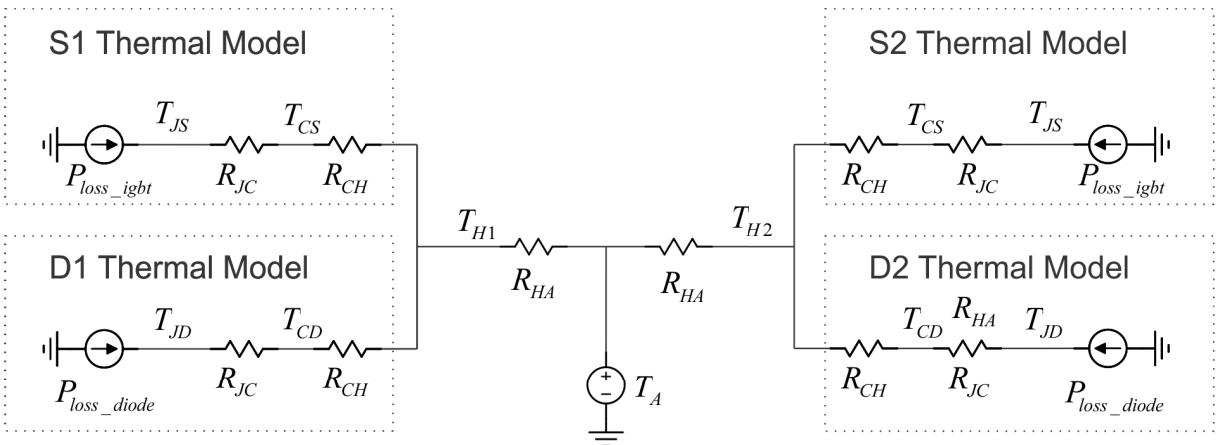
7.3.1 Losses Calculation and Junction Temperature Calculation

To calculate the junction temperature of the semiconductors, it can be used as a model wherein the total power losses are represented as a current source; the thermal resistances as Ohm resistances; and the temperature ambient as a voltage source. The current flowing through resistance will create a voltage drop on it, so the junction temperature will be the ambient temperature plus all voltage drops on the resistances.

From the topology of Figure 7.3, where each switching cell is placed on a different heatsink, the thermal model of Figure 7.4 is obtained.

- P_{loss_igbt}: Total power losses of the IGBT in W;
- P_{loss_diode}: Total power losses of the Diode in W;
- R_{JC}: Junction to Case Thermal Resistance, in °C/W;
- R_{CH}: Case to Heatsink Thermal Resistance, in degrees °C/W;
- R_{HA}: Heatsink to Ambient Thermal Resistance, in degrees °C/W;
- T_{JS}: IGBT Junction Temperature, in °C;
- T_{CS}: IGBT Case Temperature, in °C;
- T_{H1}: Heatsink 1 Temperature, in °C;
- T_{H2}: Heatsink 2 Temperature, in °C;
- T_A: Ambient Temperature, in °C.

Figure 7.4 – Converter Thermal Model



Source: Own Elaborated

It can be seen that the major junction temperature increase is by its own losses. But the heatsink temperature elevation will depend on all the looses of the semiconductors placed on it. In conclusion, one semiconductor can collaborate with the temperature elevation of another semiconductor placed on the same heatsink.

Once known the thermal model of the system, it must be calculated the losses in each semiconductor. The losses in the IGBT can be calculated as the sum of the conduction and switching losses:

$$P_{losses_igbt} = P_{cond_igbt} + P_{sw_igbt} \tag{7.5}$$

Wherein:

$$P_{cond_igbt} = V_{CE}\left(I_C\right) \cdot I_C \cdot D \tag{7.6}$$

And:

$$P_{sw_igbt} = \left(E_{on} + E_{off}\right) \cdot f_{sw} \tag{7.7}$$

$V_{CE}\left(I_C\right)$ is the voltage drop on the IGBT when it is conducting the current I_C. E_{on} is the energy loss when the IGBT starts conducting, and E_{off} is the energy loss when the IGBT is blocked. The term f_{sw} is the switching frequency.

The total diode losses are the result of conduction and switching losses:

$$P_{losses_diode} = P_{cond_diode} + P_{sw_diode} \tag{7.8}$$

Where:

$$P_{cond_diode} = V_F\left(I_C\right) \cdot I_C \cdot \left(1 - D\right) \tag{7.9}$$

And:

$$P_{sw_diode} = E_{rr} \cdot f_{sw} \tag{7.10}$$

The $V_F\left(I_C\right)$ is the forward voltage drop on the diode when it is conducting the current I_C. E_{rr} is the energy loss for reverse recovery of the diode.

According to (BARBI, 2014, p.159), the power losses due reverse recover energy on diode can be calculated as:

$$P_{rr} = \frac{t_{rr} \cdot I_{rr} \cdot E \cdot f}{3} \tag{7.11}$$

The equation (7.11) was used to estimate the energy losses from datasheet.

Then, in the datasheet of the IGBT it is found the following values presented on table 7.2

Table 7.2 – IGBT and Diode Parameters

Parameter	Test Conditions	Value	Units
E_{on}	I_C = 75 A; T_J = 125 °C; V_{CC} = 600 V; R_G = 1 Ω	2.9	mJ
E_{off}	I_C = 75 A; T_J = 125 °C; V_{CC} = 600 V; R_G = 1 Ω	5.3	mJ
t_{RR}	I_{RR}= 18.2 A; T_J= 125 °C; V_{CC} = 400 V; I_F = 50 A	278	ns
V_{CE} (57.7 A)	Tj = 125 °C	1.6	V
V_F (57.7 A)	Tj = 125 °C	2.4	V
R_{JC_IGBT}	-	0.14	°C/W
R_{JC_Diode}	-	0.31	°C/W
R_{CH}	-	0.1	°C/W

Source: Extracted from component datasheet Vishay VS-GT100DA120UF

The heatsink chosen is made of aluminum and it was projected to receive a forced air of 10 m/s, which helps its cooling and reduces its thermal resistance. The thermal resistance of the heatsink achieved was 0.15 °C/W.

With all the needed data, the junction temperature will occur on the critical operation of the converter. Since it is operating as a Buck and Boost, it has two critical operation points.

For Buck mode, the critical operation happens when there is the greatest voltage difference between input and output. In other words, the input voltage is 730 V and the output is 520 V. Then, the duty cycle for this operation is 0.7123. The average current on the main inductor is 57.7 A.

Likewise, in Boost mode, the critical point is also in the greatest voltage difference between input and output. In this case, the duty cycle applied in Boost is 0.2867, for an input voltage of 520 V and an output of 730 V. The average current on the main inductor is 57.7 A.

So, the losses were calculated based on the equations (7.5) to (7.11), adjusting proportionally to operating voltage and current compared to test conditions. The results are presented in Table 7.3. Also, it is important to remember that was used diodes and IGBTs in parallel, according to Figure 7.3.

Table 7.3 – Total Losses Per IGBT and Diode

Operating Mode	Tag Name	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)	Losses Per Device (W)
Buck	**S1**	65.8	153.5	219.3	109.6
	D1	39.8	28.4	68.3	34.1
	S2	0.0	0.0	0.0	0.0
	D2	138.5	0.0	138.5	69.2
Boost	**S1**	92.3	0.0	92.3	46.2
	D1	0.0	0.0	0.0	0.0
	S2	26.6	153.5	180.1	90.0
	D2	98.6	28.4	127.1	63.5

Source: Own Elaborated

From Table 7.3 and the model presented in Figure 7.3, the calculated junction temperatures are conferred in Table 7.4. The ambient temperature considered was 60 °C.

Table 7.4 – Calculate Junction Temperatures

Operating Mode	Tag Name	Junction Temperature (°C)
Buck	**S1**	100.7
	D1	88.4
	S2	66.9
	D2	95.3
Boost	**S1**	75.7
	D1	64.6
	S2	97.0
	D2	101.4

Source: Own Elaborated

7.4 INDUCTOR

Once known the operating frequency, was determined the maximum ripple desired to the project. As the converter will operate in CCM, the minimum output current is set to 10 A. Then, the ripple current on the inductor must be 20 A.

Maximizing equations (6.8) and (5.14), which leads to same equation:

$$L_{bb} = \frac{V_{\max}}{4 \cdot \Delta i_{L_{bb}} \cdot f_S} \tag{7.12}$$

$$L_{bb} = \frac{730(V)}{4 \cdot 20(A) \cdot 20(kHz)} \tag{7.13}$$

$$L_{bb} = 456\mu H \tag{7.14}$$

The calculation of the magnetic is also presented in Annex A. It was used four inductors series-connected to reach this inductance. The material used was Mn-Zn and the core type is EE.

7.5 FILTER

To the filter calculation, it was considered the following criteria:

- ripple voltage and current for Buck mode;
- ripple voltage and current for Boost mode;
- RMS current on the capacitors.

Although the voltage ripple criterion determines the size of the capacitor, the RMS current limits informed by the manufacturer must not be exceeded.

The maximum ripple current and voltage desired are:

$$\Delta V_{C_i} = \Delta V_{C_o} = 0.02 \cdot V_{\max} = 14.6V \tag{7.15}$$

$$\Delta I_{L_i} = \Delta I_{L_o} = 0.01 \cdot I_{L_max} = 0.57A \tag{7.16}$$

7.5.1 Buck Mode

For Buck mode, the following input and output filter were found:

$$C_i = \frac{I_{L_{bb_max}}}{4 \cdot \Delta V_{C_i} \cdot f_S \cdot n^2} \tag{7.17}$$

$$C_i = 12.208\mu F \tag{7.18}$$

$$L_i = \frac{I_{L_{bb_max}}}{32 \cdot \Delta I_{L_i} \cdot f_S^2 \cdot n^3 \cdot C_i} \tag{7.19}$$

$$L_i = 80\mu H \tag{7.20}$$

$$C_o = \frac{V_{\max}}{32 \cdot \Delta V_{C_o} \cdot f_S^2 \cdot n^2 \cdot L_{bb}} \tag{7.21}$$

$$C_o = 2.14\mu F \tag{7.22}$$

$$L_o = \left(\frac{V_{\max}}{4 \cdot \Delta I_{L_o} \cdot f_S \cdot n^2} - 1 \right) \cdot \frac{1}{4\pi^2 \cdot (n \cdot f_S)^2 \cdot C_o} \tag{7.23}$$

$$L_o = 122.29\mu H \tag{7.24}$$

7.5.2 Boost Mode

For Boost mode, the following input and output filter were found:

$$C_i = \frac{V_{\max}}{32 \cdot \Delta V_{C_i} \cdot f_S^2 \cdot n^2 \cdot L_{bb}} \tag{7.25}$$

$$C_i = 2.14\mu F \tag{7.26}$$

$$L_i = \left(\frac{V_{\max}}{4 \cdot \Delta I_{L_i} \cdot f_S \cdot n^2} - 1 \right) \cdot \frac{1}{4\pi^2 \cdot (n \cdot f_S)^2 \cdot C_i} \tag{7.27}$$

$$L_i = 122.29\mu H \tag{7.28}$$

$$C_o = \frac{I_{L_{bb_max}}}{4 \cdot \Delta V_{C_o} \cdot f_S \cdot n^2} \tag{7.29}$$

$$C_o = 12.208\mu F \tag{7.30}$$

$$L_o = \frac{I_{L_{bb_max}}}{32 \cdot \Delta I_{L_o} \cdot f_S^2 \cdot n^3 \cdot C_o} \tag{7.31}$$

$$L_o = 80\mu H \tag{7.32}$$

7.5.3 RMS Current in the Capacitors

The RMS current must be calculated to find a suitable capacitor. The manufacturer tells what is the maximum allowed current to avoid overheats, increasing the capacitor lifetime.

The maximum RMS current on the input capacitor will happen in the Buck mode when the current is pulsed. On the other hand, the maximum RMS current on the output capacitor will happen when it is in Boost mode, also with pulsed currents.

For Buck mode, in the first interval from 0 to DT_S, the switch is closed. So, the current on the capacitor is:

$$I_{in} = I_{C_i} + I_L \tag{7.33}$$

Then:

$$I_{C_i} = I_{in} - I_o \tag{7.34}$$

$$I_{C_i} = \frac{P_o}{V_{in}} - \frac{P_o}{V_o} \tag{7.35}$$

And for the interval from DT_S to $(1-D)T_S$, when the switch is open, the current on the capacitor is:

$$I_{C_i} = I_{in} \tag{7.36}$$

Or:

$$I_{C_i} = \frac{P_o}{V_{in}} \tag{7.37}$$

Then, the RMS current is given by:

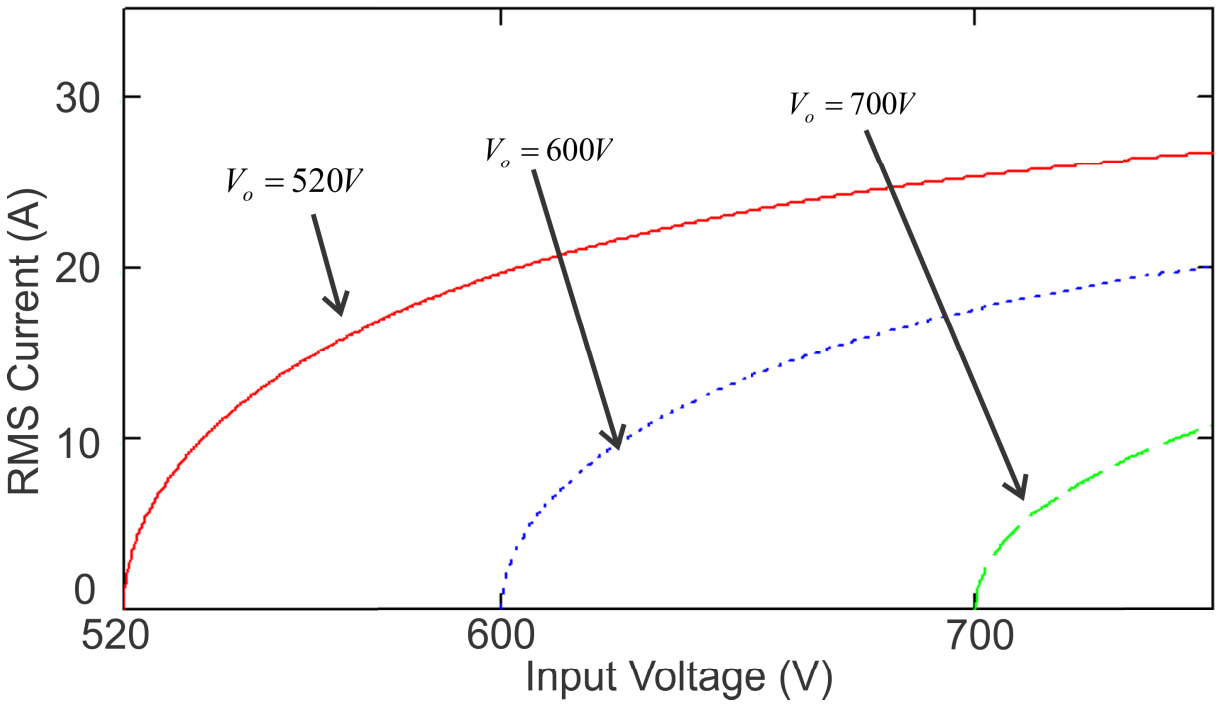
$$I_{C_i_rms} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_{C_i}(t) \cdot dt} \tag{7.38}$$

Solving equation (7.38):

$$I_{C_i_rms} = P_o\sqrt{\frac{1}{V_o V_{in}} - \frac{1}{V_{in}^2}} \tag{7.39}$$

It can be seen that as close as V_o is to V_{in}, the RMS current is lower. Then, the maximum RMS current is in the greatest voltage difference. Figure 7.5 shows the RMS current, given the input and output voltage.

Figure 7.5 – RMS Current in Input Capacitor C_i



Source: Own elaborated

Therefore, the maximum RMS current of the capacitor occurs for $V_{in} = 730V$ and $V_o = 520V$:

$$I_{C_{i_rms}} = 26.116A \tag{7.40}$$

The calculation for the output capacitor is done to Boost mode. In the interval from 0 to DT_S, the capacitor current is:

$$I_{C_o} = -I_o \tag{7.41}$$

Or:

$$I_{C_o} = -\frac{P_o}{V_o} \tag{7.42}$$

For the interval from DT_S to $(1-D)T_S$, the current on the capacitor is:

$$I_{C_o} = I_L - I_o \tag{7.43}$$

Then:

$$I_{C_o} = I_{in} - I_o \tag{7.44}$$

Or:

$$I_{C_o} = \frac{P_o}{V_{in}} - \frac{P_o}{V_o} \tag{7.45}$$

The RMS current can be calculated as:

$$I_{C_{o_rms}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_{C_o}(t) \cdot dt} \tag{7.46}$$

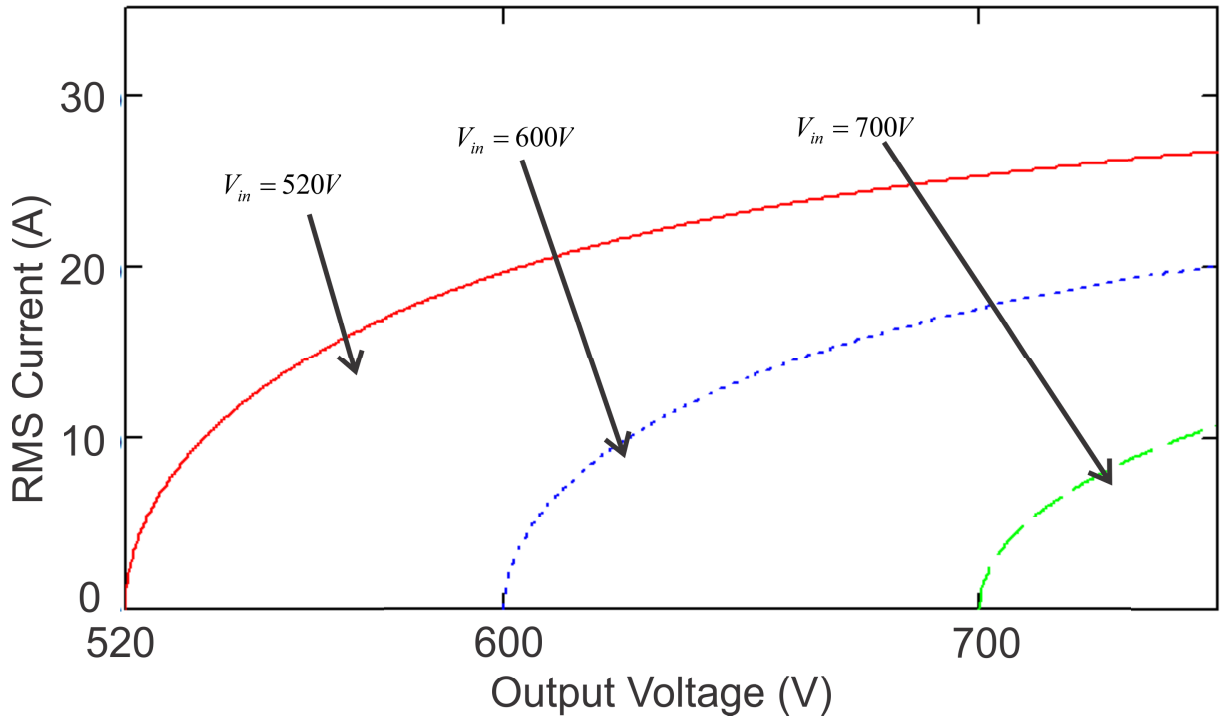
Solving equation (7.46):

$$I_{C_{o_rms}} = P_o\sqrt{\frac{1}{V_o V_{in}} - \frac{1}{V_o^2}} \tag{7.47}$$

Thence, the maximum RMS current will occur when the voltage difference between the input and the output is the larger, as seen in Figure 7.6.

Figure 7.6 shows the RMS current in the input capacitor for different input voltages.

Figure 7.6 – RMS Current in Output Capacitor C_o



Source: Own elaborated

The maximum RMS current of the input capacitor happens for V_o = 730 V and V_{in} 520 V:

$$I_{C_o_rms} = 26.116A \tag{7.48}$$

Given these values, it was used six strings of two capacitors series-connected of $2400\mu F$, giving a capacitance of $7200\mu F$. This arrangement of capacitors was used for the input and the output.

It is important to remember that the equations used to calculate the RMS current are valid for low ripple current on the inductors, once that was considered just the average component of the currents.

Then, the output inductor was calculated based on the worst operation scenario: Buck mode for the input and Boost mode for the output.

$$C_i = C_o = 7200\mu F \tag{7.49}$$

$$L_i = \frac{I_{L_{bb_max}}}{32 \cdot \Delta I_{L_i} \cdot f_S^2 \cdot n^3 \cdot C_i} \tag{7.50}$$

$$L_i = 136nH \tag{7.51}$$

$$L_o = \frac{I_{L_{bb_max}}}{32 \cdot \Delta I_{L_o} \cdot f_S^2 \cdot n^3 \cdot C_o} \tag{7.52}$$

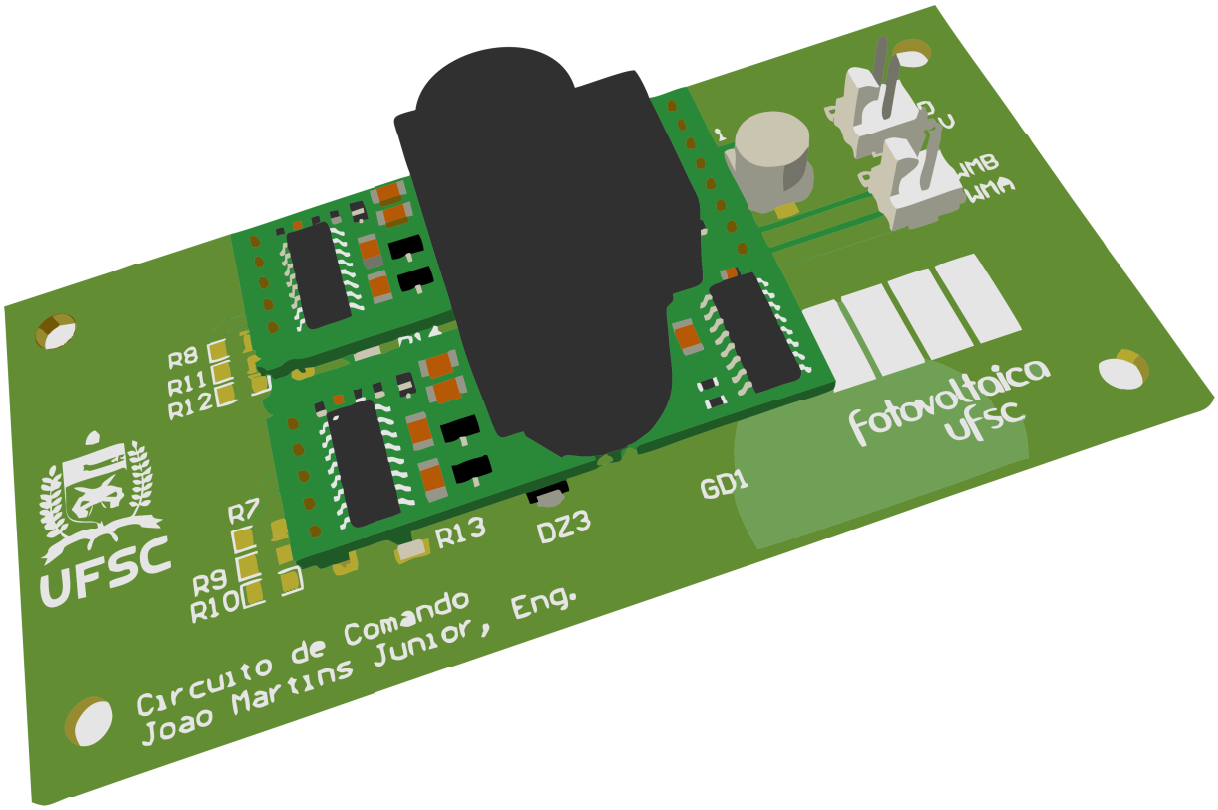
$$L_o = 136nH \tag{7.53}$$

The values of the input and output of the inductor are in the range of nano Henrys. To have an idea about inductance values of a copper wire cable, one meter with a 25 squared millimeter section has about 500 nH of inductance (measured in Fotovoltaica laboratory). So, for this project, it was not designed inductors for input and output, once that the inductance of the cables used to connect the converter is sufficient to produce higher inductances than required.

7.6 GATE DRIVER

The gate driver must be used to provide an isolated PWM signal at the gate of each IGBT. The gate driver used was from Power Integration manufacturer, model 2SC0106T. An interface board was used to place the gate resistors, the TVS diodes for protection, and the connectors to receive the PWM signal from the mainboard and the power supply. This is shown in Figure 7.7.

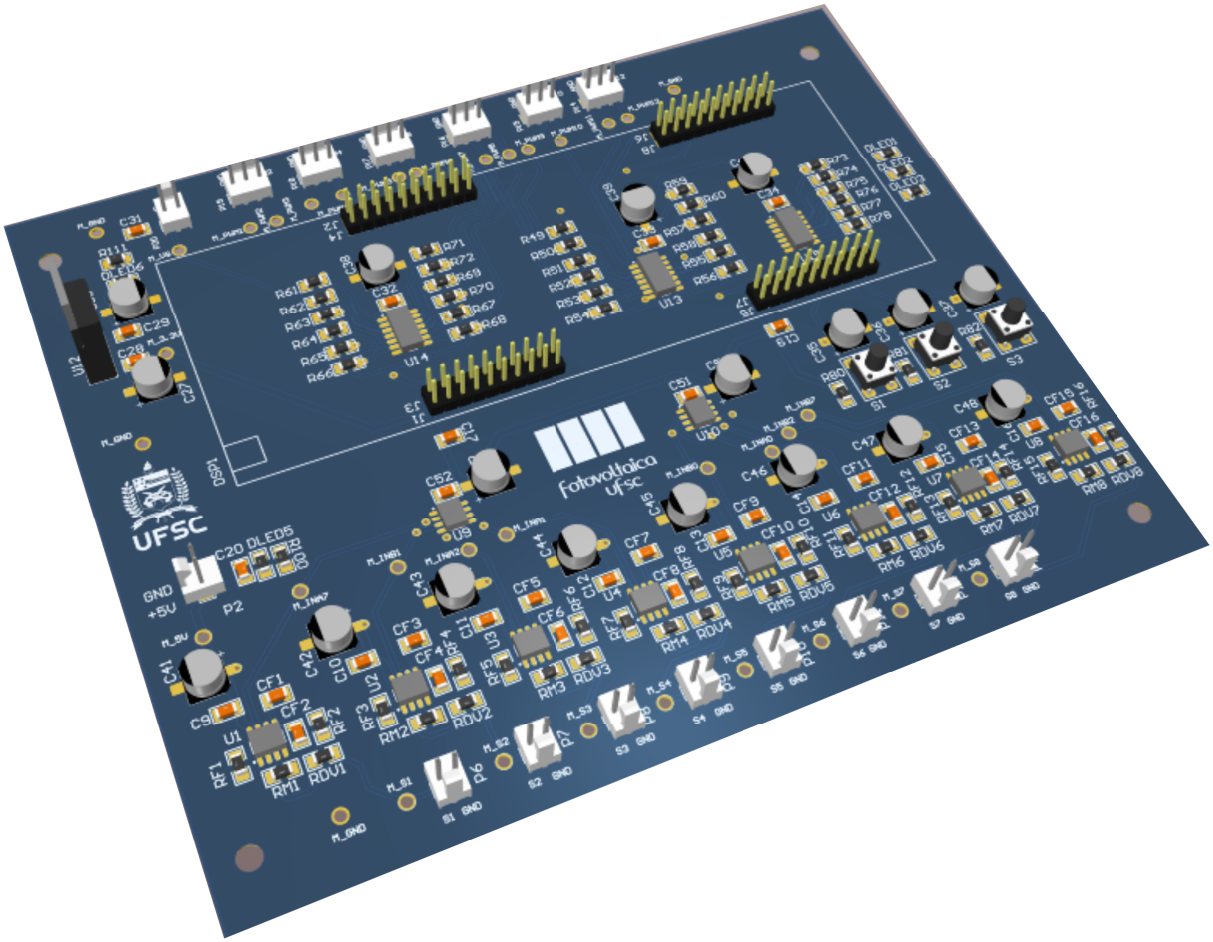
Figure 7.7 – Gate Driver



7.7 CONTROL BOARD

The control board used was designed by the standard used by the Fotovoltaica research group. All the signal processing was personalized given the requirements of the project. The microcontroller used to signal processing and the command PWM was the launchpad LAUNCHXL-F28069M from Texas Instruments. The processor has a clock of 90 MHz, allowing digital control of the converter. The board is presented in Figure 7.8.

Figure 7.8 – Control Board



7.8 TRANSDUCERS

It was used two types of transducers:

- Voltage Transducer LV-25P/SP5 from LEM: this is a transducer which measures the voltage through hall effect. Providing a parallel resistance with the voltage to

be read, it draws a small current which is proportional to the voltage. The output is given in Volts.

- Current Transducer HASS 100-S: this is a sensor that measures the current through hall effect. Its output is given in Volts.

7.9 ASSEMBLY

The converter was designed with air-cooled modules. It was not designed PCBs for the energy conversion side due to its power rate. To connect IGBTs, inductors, and capacitors, it was used copper bars.

Figures 7.9, 7.10, and 7.11 shows pictures of the final assembly of the converter.

Figure 7.9 – Perspective view of the Converter

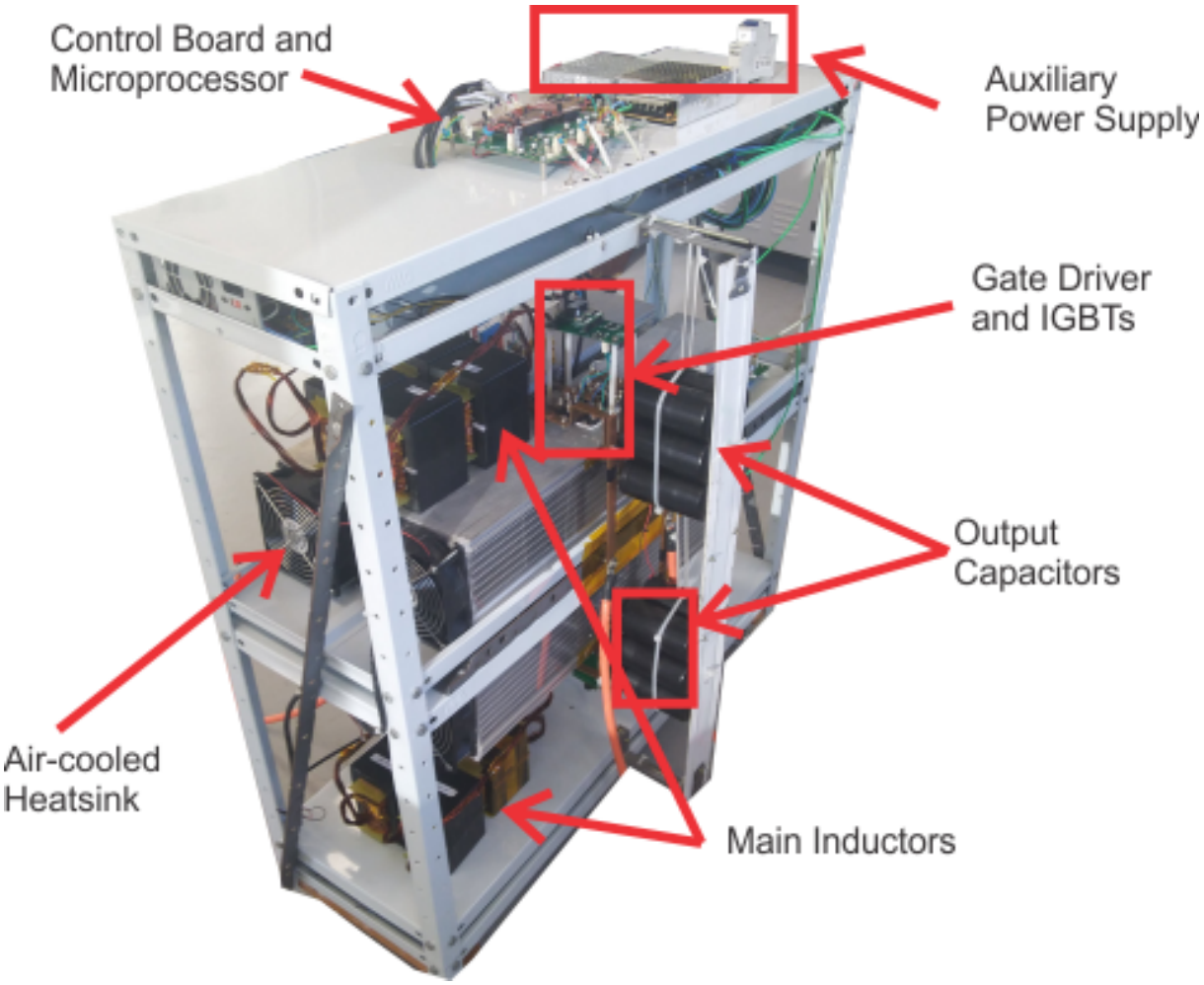


Figure 7.10 – Frontal view of the Converter

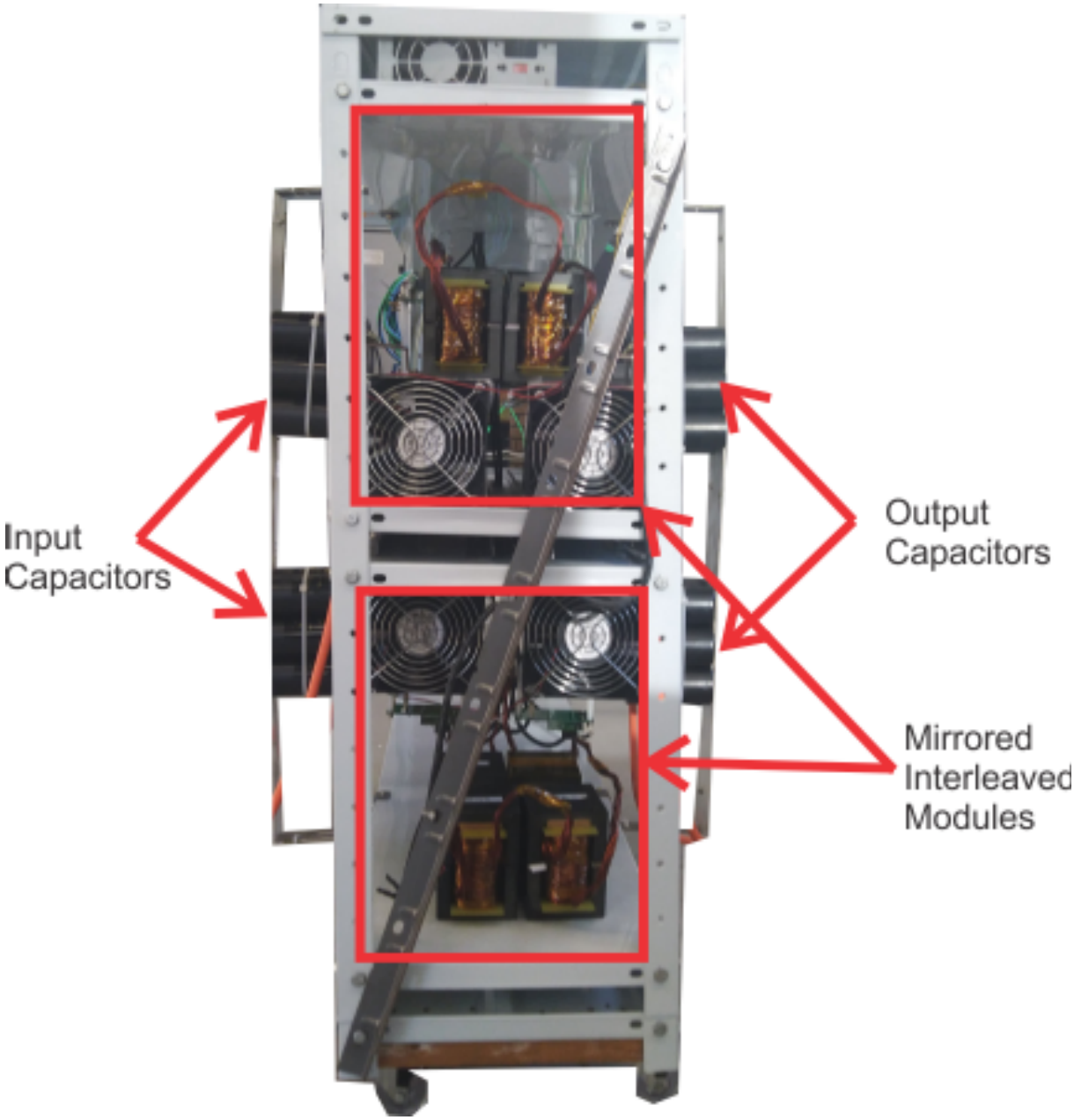
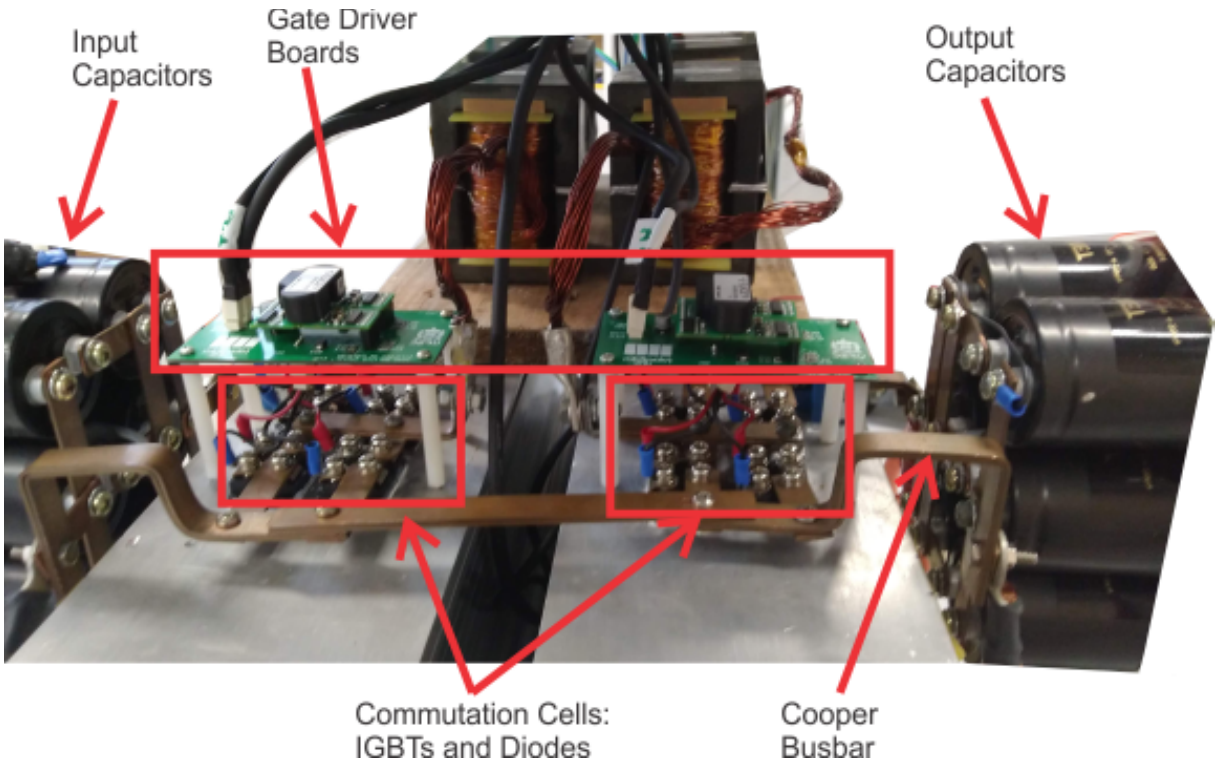


Figure 7.11 – Internal view of the Converter



7.10 PARTIAL CONCLUSIONS

The converter design is one of the most time-consuming in the whole study. Each component must be carefully chosen to avoid operating issues. Besides its complexity, on this step, the power electronics start to get a physical form.

From the size of the built converter exhibited in Figures 7.9, 7.10, and 7.11, it can be inferred that there was a lot of mechanical work. The design was done to place filter capacitors as close as possible from commutation cells. Also, it is important to place the gate drivers close to the IGBT to avoid EMI interference.

8 DROOP CONTROL WITH VIRTUAL RESISTANCES

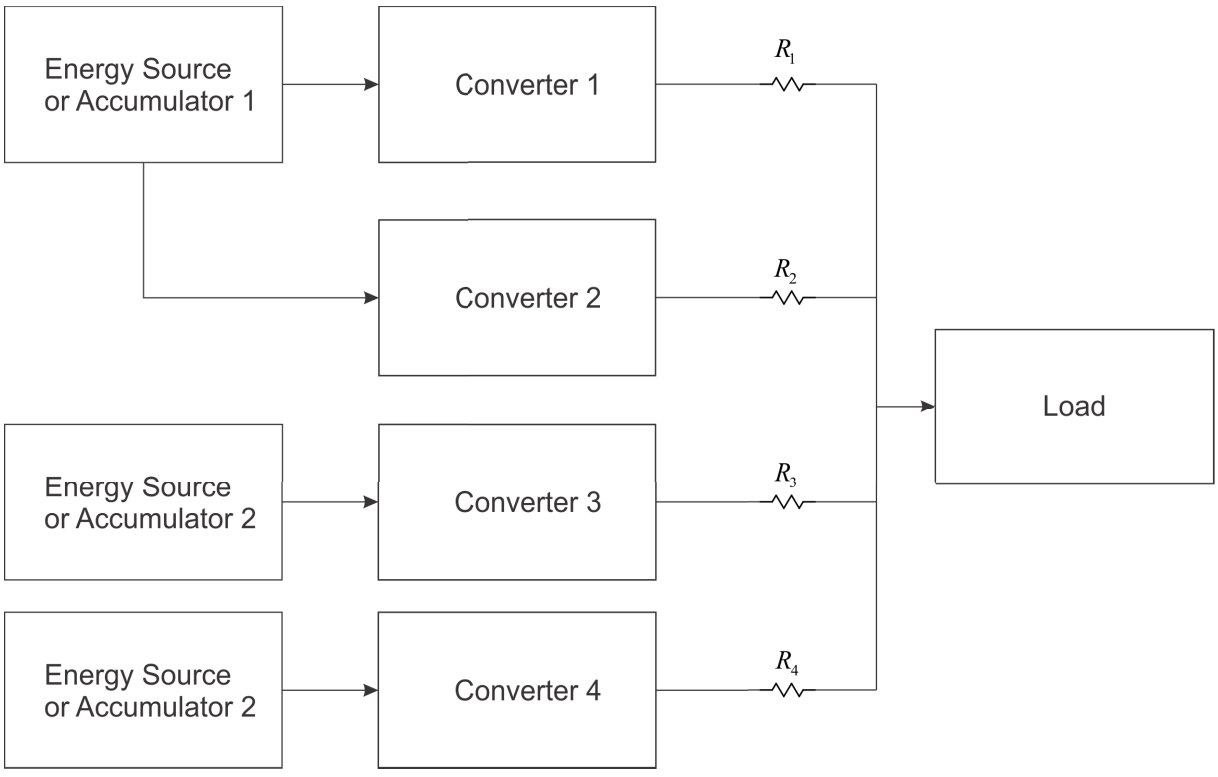
Paralleling modules can be classified into two categories: droop methods and active current sharing methods. The droop method consists of setting an output impedance for the system to achieve current sharing, while current sharing methods can be deemed as the inclusion of an outer control loop (SHIGUO LUO et al., 1999).

8.1 DROOP CONTROL

Droop control methods are being popularized due to the increase of distributed generation, as they do not need communication among converters. They can be used to integrate diesel generators with batteries and photovoltaic energy as shown in (SUSE-TYO et al., 2017). They also can be used to control the power flow of distinct battery banks, shown by (LEAL, 2017).

The droop control requires an impedance on the output of the converter, which will regulate its output current. This means that the converters can be seen as a voltage source, and their output current is limited by the load; their own series resistance; and their interaction with other resistors, as shown in Figure 8.1. The energy source of each converter can be shared or independent.

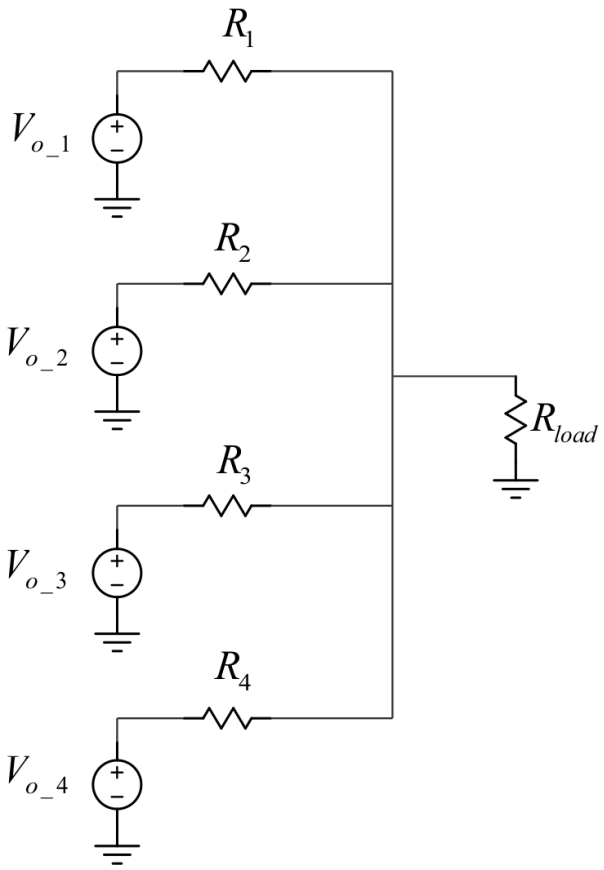
Figure 8.1 – Droop Structure



Source: Own elaborated

According to the output voltage of each converter and its resistance, it is possible to control the power flow of each converter. The electrical model of Figure 8.1 is shown in Figure 8.2, wherein V_{o_x} represents the equivalent output voltage of each converter.

Figure 8.2 – Droop Structure Electrical Model

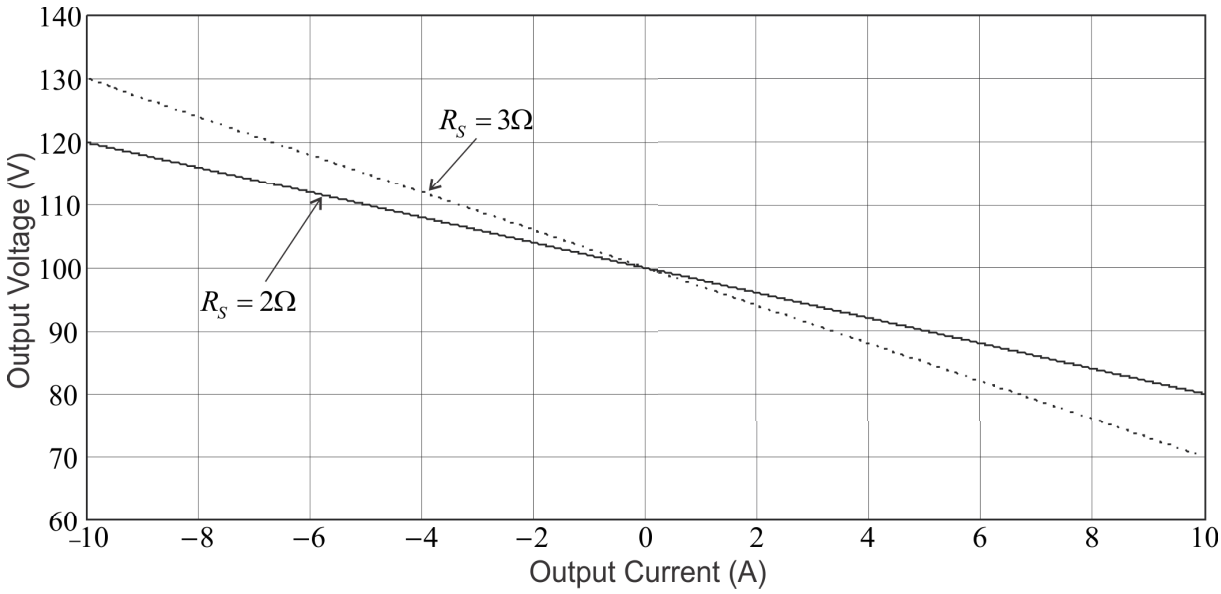


Source: Own elaborated

It can be seen from Figure 8.2 that if all the output voltages and resistances are the same, the current will be equal among the converters. Also can be noted that, in the droop method, the load voltage regulation will depend on the parameters of the system and the load itself.

Figure 8.3 presents the output characteristics of an electrical voltage source in series with a resistance. In this case, the voltage source is 100 V for two different resistances: 2 and 3 Ω. If the current is drawn from the voltage source, there is a voltage drop in the load, which is proportional to the output current and the resistance.

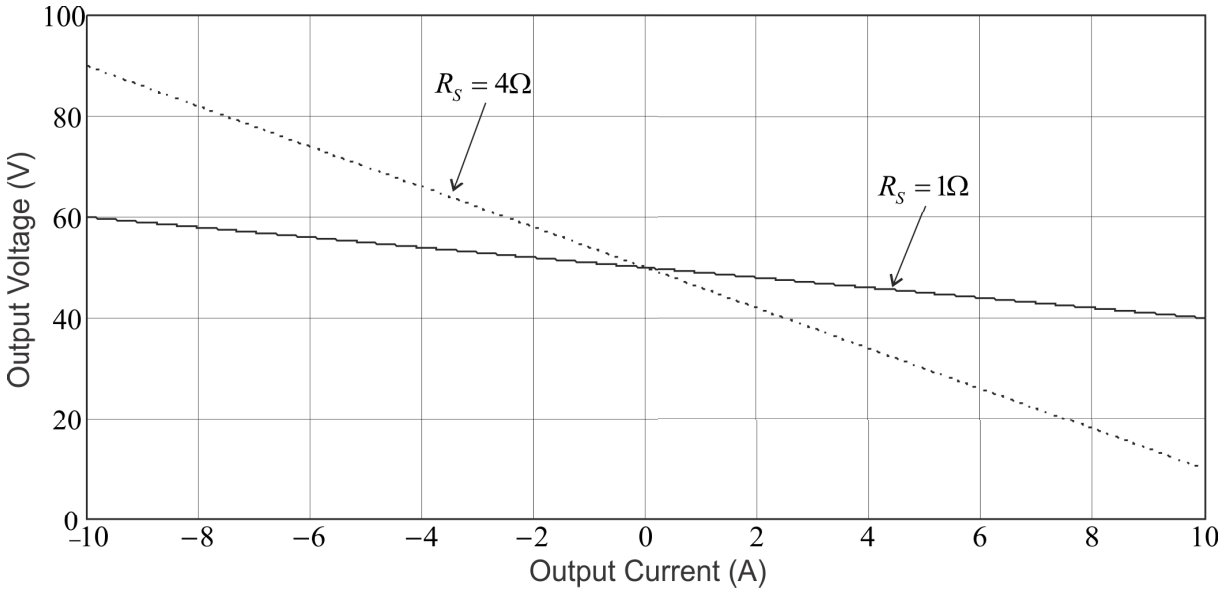
Figure 8.3 – Output Characteristic 1



Source: Own elaborated

Similarly in Figure 8.4, there is a voltage source of 50 V for two different resistances in series: 1 and 4 Ω. The smaller is the series resistance, the less output voltage will change.

Figure 8.4 – Output Characteristic 2



Source: Own elaborated

Figure 8.5 shows two voltage sources with equal series resistance. It also presents its equivalent Thevenin model. Figure 8.6 exhibits the $I_o x V_o$ curves for each

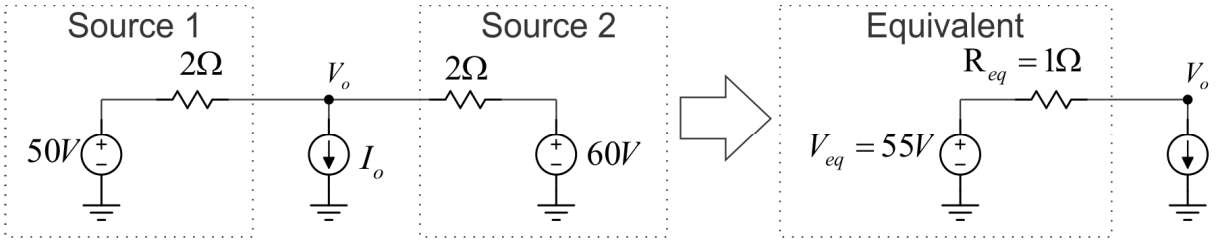
voltage source.

If the current source is I_o is 35 A, the output voltage V_o can be calculated as:

$$V_o = 55 - 35 \cdot 1 = 20 \tag{8.1}$$

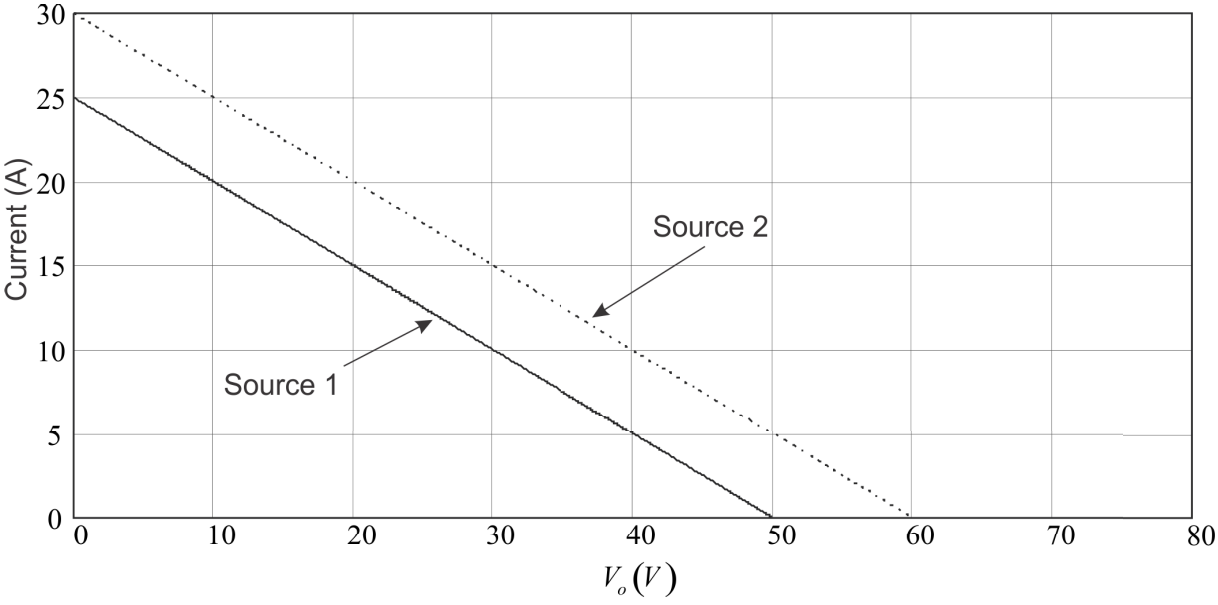
In this condition, the current in the Source 1 is 15 A, while in Source 2 is 20 A, as shown in Figure 8.6. The consequence of the equal series resistance of each voltage source is that the current in the Source 2 will be always greater than the current in Source 1. It can be easily understood, once that the series resistances are equal, and the voltage Source 2 has a greater voltage than 1.

Figure 8.5 – Droop 1



Source: Own elaborated

Figure 8.6 – Droop 1 Curves

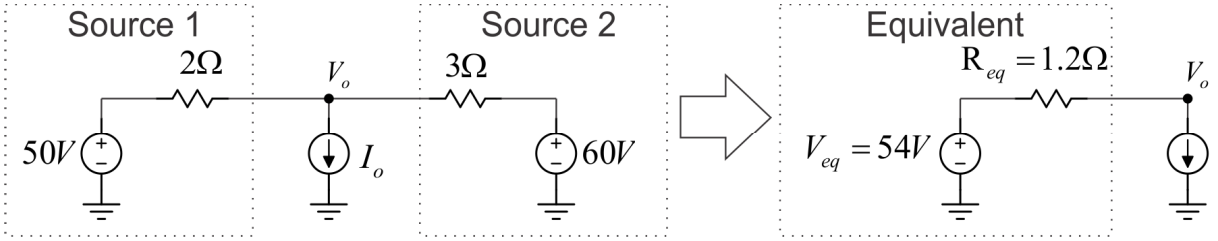


Source: Own elaborated

The current for V_o equal zero of each source is the short circuit current of the source and the voltage for no current sink is the open-circuit voltage.

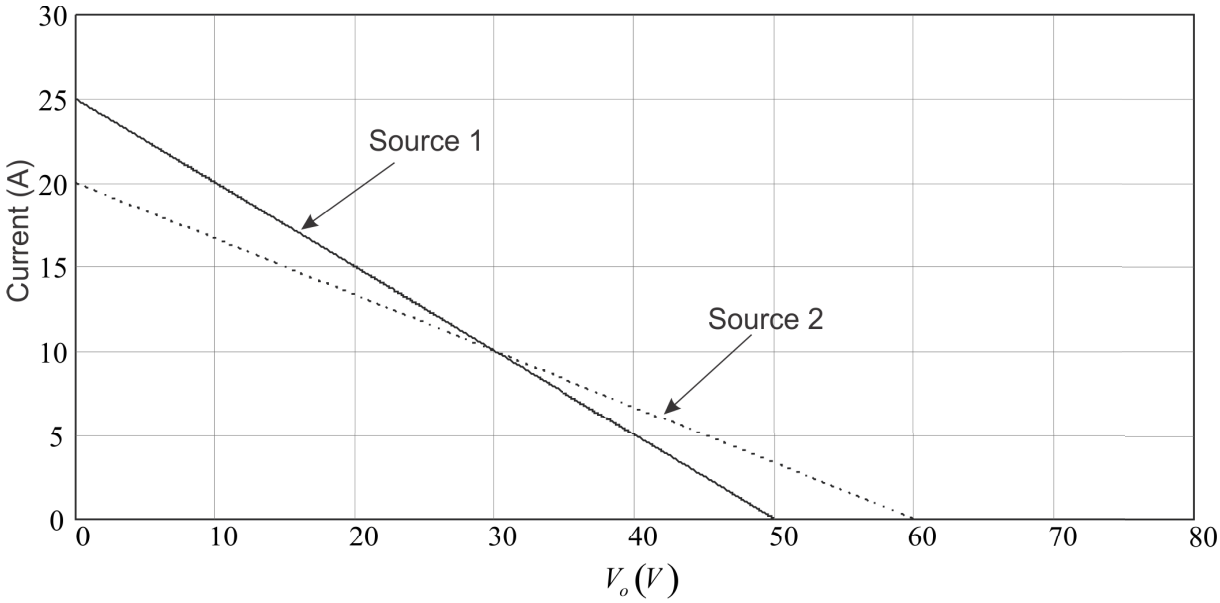
Figure 8.7 presents an electrical system with two different voltage sources and resistances. The consequence of different resistance will reflect on different angular coefficients. In other words, the curves will have an intersection point, changing the current distribution among the sources.

Figure 8.7 – Droop 2



Source: Own elaborated

Figure 8.8 – Droop 2 Curves

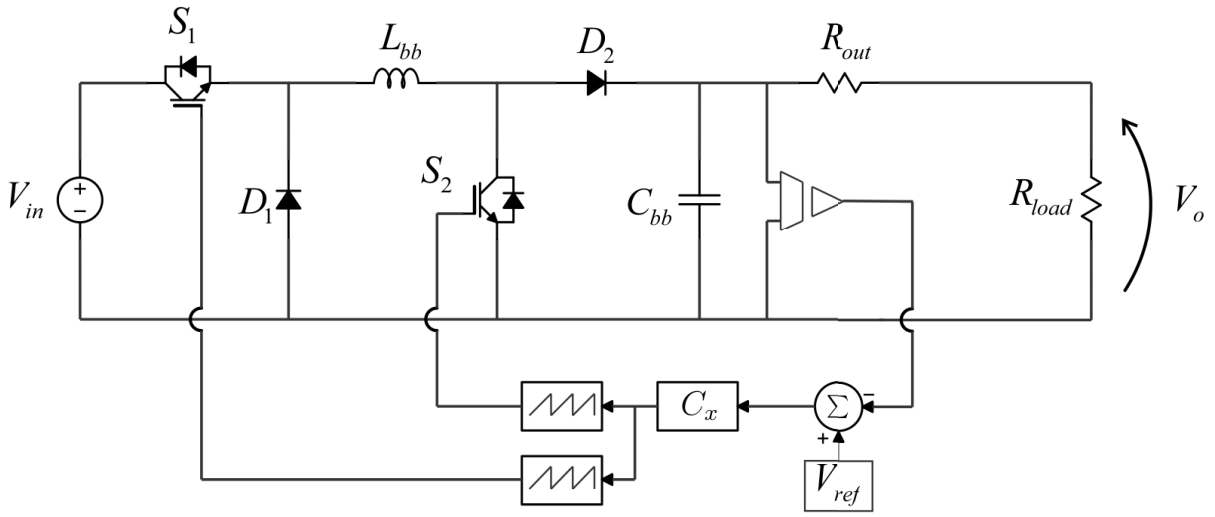


Source: Own elaborated

Then, the droop control is a technique wherein the combination of output voltage and resistance defines the current distribution in integrated systems, without the need for communication. Once it is possible to control the output voltage in static converters, this method can be applied to share currents in parallel converters.

Figure 8.9 presents the control scheme of Non-Inverter Buck-Boost. Once controlled the output voltage, it is possible to implement droop control with the addition of an output series resistance R_{out}. However, the output resistance will reduce the global efficiency of the converter.

Figure 8.9 – NIBB Output Voltage Control

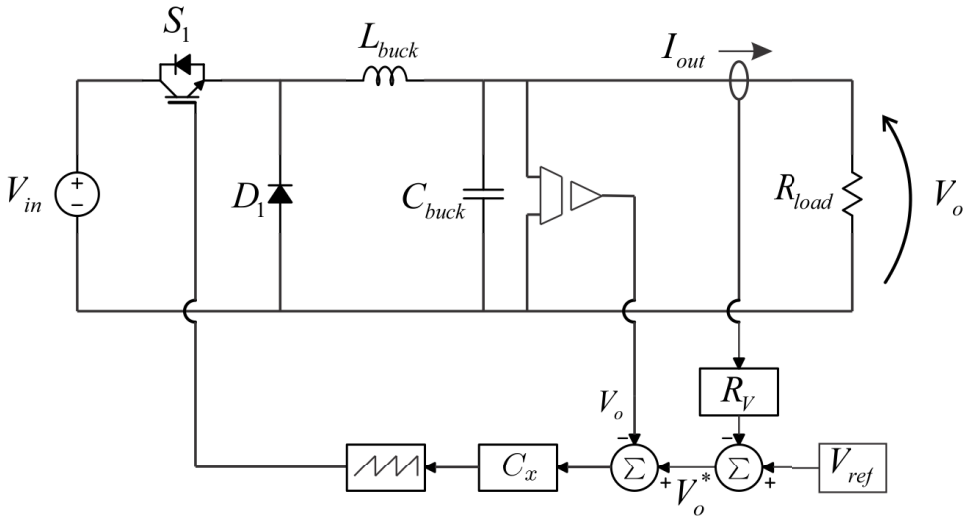


Source: Own elaborated

8.2 VIRTUAL RESISTANCES

Virtual resistances can be understood as an introduction, by the control loop, of a resistance characteristic in a converter. They can be used to stabilize the converter in a dynamic view, and also can be used to implement droop control. Figure 8.10 presents a Buck converter with an input filter, wherein a virtual resistance is created by measuring the output current.

Figure 8.10 – Buck with virtual resistance



Source: Own elaborated

The compensated output voltage presented in Figure 8.10 can be expressed as:

$$V_o = V_{ref} - R_V \cdot I_{out} \tag{8.2}$$

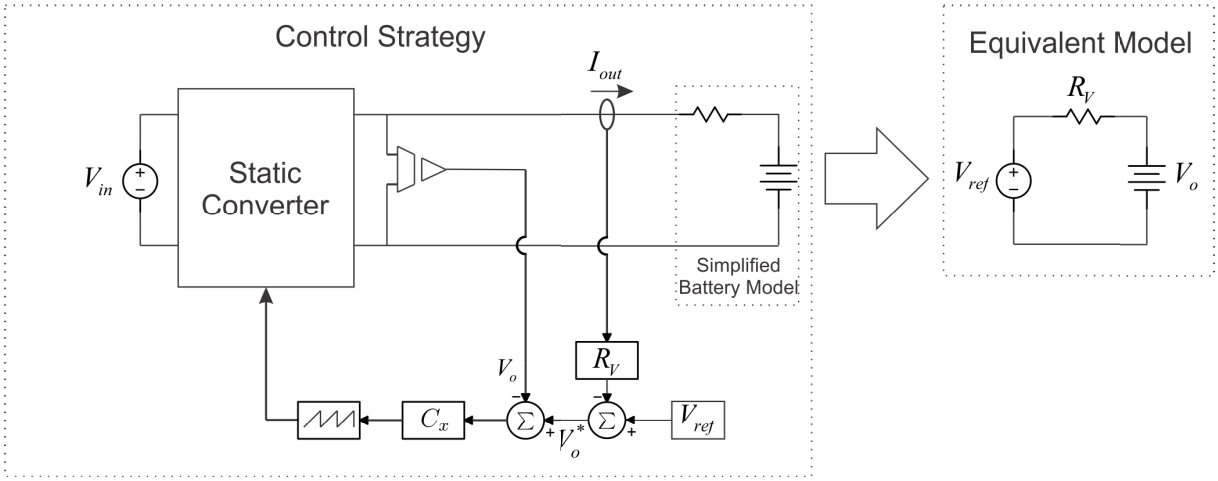
Then, including the current measurement to define the output reference voltage will cause the same effect as a physical resistance on the output, without consuming any energy. Also, virtual resistances can be easily configured in digital controlled converters.

8.3 CONTROL STRATEGY

The droop control now can be applied to the designed NIBB. Therefore, the implementation of the battery is not trivial. The output voltage for resistive loads will be defined with the equalization of the system and all the converters. Batteries will set the output voltage.

Figure 8.11 shows the control strategy applied to batteries and its equivalent circuit. The resultant model shows that if V_{ref} and R_V are constants, then the output current will be defined by the battery voltage, that is, by the current State of Charge.

Figure 8.11 – Charging Batteries with Droop Control



Source: Own elaborated

The consequence of the battery voltage defining the output current is that the constant current constant voltage charging method is not feasible. The studied battery bank can reach 730 V and its minimum voltage is 526 V. Also, the maximum output current is 400 A. So, the minimum virtual resistance can be calculated as:

$$R_{V_min} = \frac{730V - 526V}{400A} = 0.51\Omega \tag{8.3}$$

Considering that this current is for 10 paralleled modules, the minimum virtual resistance of each converter is:

$$R_{V_min} = 5.1\Omega \tag{8.4}$$

It can be inferred that the charging current will be 400 A only when the input voltage is 730 V and the output voltage is 526 V. Any other condition, the current will be lower.

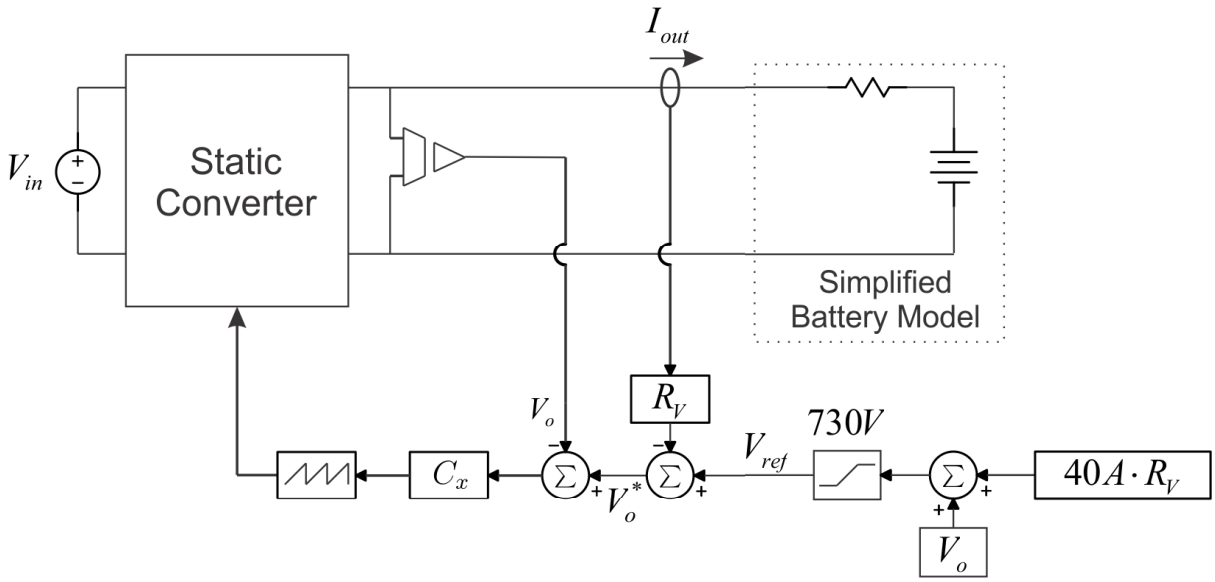
To achieve the constant current constant voltage method, modifications to the control strategy are necessary. During the constant current interval, the reference voltage must be defined to limit the output current. During the constant voltage interval, the reference voltage is fixed and the current will start dropping according to the SoC of the batteries.

Figure 8.12 shows the condition for the designed converter to operate. It can be mathematically expressed by the equations:

$$V_{ref} = V_o + R_V \cdot 40A \tag{8.5}$$

$$V_o = V_{ref} - R_V \cdot I_{out} \tag{8.6}$$

Figure 8.12 – Modified Droop Control for Constant Current Constant Voltage Charging Method



Source: Own elaborated

When $V_o + R_V \cdot 40A$ is less than 730 V, the output current can be calculated applying the equation (8.5) in (8.6), which will result I_{out} equal 40 A, performing the constant current charging method.

When $V_o + R_V \cdot 40A$ results in more than 730 V, V_{ref} will be fixed in 730 V. Then, the output current will be defined by the battery voltage. As the battery voltage is increasing, the output current is being automatically reduced, performing the constant voltage charging method.

Then, the control strategy presented in Figure 8.12 is implemented in the system architecture. Then, it is necessary to find the converter dynamical plant to calculate properly the compensator C_x.

Another approach to control the NIBB converter can be verified in (NICOLLI, 2019), where it is used a current control loop in cascade with a voltage control loop.

8.4 DYNAMICAL MODELING

The dynamical model of the converter is important to design safely the controller. In practice, it means that the dynamic model is necessary for stable operation of the converter. Once the system proposed is composed of batteries, a controller is mandatory in the project.

The proposed controller will read the output voltage and output current, to implement the virtual resistance. To model the converter, it is considered that the converter is operating in CCM. Also, it is considered the parasite resistance in the inductors.

8.4.1 State Space Model

One way to extract the dynamic characteristics of the converter is using the State Space Model (SSM). To do that, it is needed the equations which describe the converter in each topological state. The average model of the converter can be obtained from:

$$K = K_1 \cdot D + K_2 \cdot (1 - D) \tag{8.7}$$

$$A = A_1 \cdot D + A_2 \cdot (1 - D) \tag{8.8}$$

$$B = B_1 \cdot D + B_2 \cdot (1 - D) \tag{8.9}$$

$$C = C_1 \cdot D + C_2 \cdot (1 - D) \tag{8.10}$$

$$E = E_1 \cdot D + E_2 \cdot (1 - D) \tag{8.11}$$

Also, if consider $(1 - D) = D'$:

$$K = K_1 \cdot D + K_2 \cdot D' \tag{8.12}$$

$$A = A_1 \cdot D + A_2 \cdot D' \tag{8.13}$$

$$B = B_1 \cdot D + B_2 \cdot D' \tag{8.14}$$

$$C = C_1 \cdot D + C_2 \cdot D' \tag{8.15}$$

$$E = E_1 \cdot D + E_2 \cdot D' \tag{8.16}$$

Wherein:

- **A** is the state matrix;
- **B** is the input matrix;
- **C** is the output matrix;
- **D** is the duty cycle;
- **D** is the complementary duty cycle;
- **E** is the feedthrough matrix;
- **K** is a constant matrix;
- **A1** is the state matrix for the first topological state;
- **B1** is the input matrix for the first topological state;
- **C1** is the output matrix for the first topological state;
- **E1** is the feedthrough matrix for the first topological state;
- **K1** is a constant matrix for the first topological state;
- **A2** is the state matrix for the second topological state;
- **B2** is the input matrix for the second topological state;
- **C2** is the output matrix for the second topological state;
- **E2** is the feedthrough matrix for the second topological state;
- **K2** is a constant matrix for the second topological state;

Applying small perturbations on the input variables, it is found:

$$x = X + \hat{x} \tag{8.17}$$

$$u = U + \hat{u} \tag{8.18}$$

$$d = D + \hat{d} \tag{8.19}$$

$$d' = D' - \hat{d} \tag{8.20}$$

$$y = Y + \hat{y} \tag{8.21}$$

Wherein:

- **x** is the perturbed state vector;

- **u** is the perturbed input vector;
- **d** is the perturbed duty cycle;
- **d'** is the perturbed complementary duty cycle;
- **y** is the output vector;
- **X** is the state vector;
- **U** is the input vector;
- **Y** is the output vector;
- $\hat{x}$ is the perturbation in the state vector;
- $\hat{u}$ is the perturbation in the input vector;
- $\hat{d}$ is the perturbation in the duty cycle;
- $\hat{y}$ is the perturbation in the output vector;

Considering that the uppercase letters represent the steady-state of the converter and lowercase letters with a hat represents the input perturbations of the system, then the perturbed average model is:

$$K \cdot \dot{\hat{x}} = A \cdot x + B \cdot u \tag{8.22}$$

$$\begin{aligned} &\left[K_1 \cdot \left(D + \hat{d}\right) + K_2 \cdot \left(D - \hat{d}\right)\right] \cdot \left(\dot{X} + \dot{\hat{x}}\right) = \\ &= \left[A_1 \cdot \left(D + \hat{d}\right) + A_2 \cdot \left(D - \hat{d}\right)\right] \cdot (X + \hat{x}) + \\ &+ \left[B_1 \cdot \left(D + \hat{d}\right) + B_2 \cdot \left(D - \hat{d}\right)\right] \cdot (U + \hat{u}) \end{aligned} \tag{8.23}$$

$$\begin{aligned} Y + \hat{y} = &\left[C_1 \cdot \left(D + \hat{d}\right) + C_2 \cdot \left(D - \hat{d}\right)\right] \cdot (X + \hat{x}) + \\ &+ \left[E_1 \cdot \left(D + \hat{d}\right) + E_2 \cdot \left(D - \hat{d}\right)\right] \cdot (U + \hat{u}) \end{aligned} \tag{8.24}$$

Considering that:

$$A_d = A_1 - A_2 \tag{8.25}$$

$$B_d = B_1 - B_2 \tag{8.26}$$

$$C_d = C_1 - C_2 \tag{8.27}$$

$$E_d = E_1 - E_2 \tag{8.28}$$

$$K_1 = K_2 \tag{8.29}$$

Adjusting the terms and considering the equations (8.7) to (8.11), it is found:

$$\begin{aligned} K \cdot \hat{\dot{x}} = & \underbrace{A \cdot X + B \cdot U}_{CC\ terms} + \\ & + \underbrace{(A_d \cdot X + B_d \cdot U) \cdot \hat{d} + A \cdot \hat{x} + B \cdot \hat{u}}_{1^{\text{st}}\ order\ terms} + \\ & + \underbrace{A_d \cdot \hat{d} \cdot \hat{x} + B_d \cdot \hat{d} \cdot \hat{u}}_{2^{\text{nd}}\ order\ terms} \end{aligned} \tag{8.30}$$

$$\begin{aligned} Y + \hat{y} = & \underbrace{C \cdot X + E \cdot U}_{CC\ terms} + \\ & + \underbrace{(C_d \cdot X + E_d \cdot U) \cdot \hat{d} + C \cdot \hat{x} + E \cdot \hat{u}}_{,1^{\text{st}}\ order\ terms} + \\ & + \underbrace{C_d \cdot \hat{d} \cdot \hat{x} + E_d \cdot \hat{d} \cdot \hat{u}}_{2^{\text{nd}}\ order\ terms} \end{aligned} \tag{8.31}$$

From CC terms, it is possible to find the steady-state output, described by:

$$0 = A \cdot X + B \cdot U \tag{8.32}$$

$$Y = C \cdot X + E \cdot U \tag{8.33}$$

Therefore:

$$X = -A^{-1} \cdot B \cdot U \tag{8.34}$$

Then:

$$Y = C \cdot \left(-A^{-1} \cdot B \cdot U\right) + E \cdot U \tag{8.35}$$

Considering:

$$\begin{aligned} F_d &= (A_d \cdot X + B_d \cdot U) \\ G_d &= (C_d \cdot X + E_d \cdot U) \end{aligned} \tag{8.36}$$

The desired plants can be obtained from the first-order elements, that is:

$$K \cdot \hat{\dot{x}} = A \cdot \hat{x} + F_d \cdot \hat{d} + B \cdot \hat{u} \tag{8.37}$$

$$\hat{y} = C \cdot \hat{x} + G_d \cdot \hat{d} + E \cdot \hat{u} \tag{8.38}$$

Applying Laplace transform:

$$\begin{aligned} K \cdot s \cdot X(s) &= A \cdot X(s) + F_d \cdot D(s) + B \cdot U(s) \\ Y(s) &= C \cdot X(s) + G_d \cdot D(s) + E \cdot U(s) \end{aligned} \tag{8.39}$$

Therefore $X(s)$ can be calculated as:

$$X(s) = (K \cdot s - A)^{-1} \cdot [F_d \cdot D(s) + B \cdot U(s)] \tag{8.40}$$

And the output as:

$$Y(s) = \left[C(Ks - A)^{-1}\right] \cdot [F_d D(s) + BU(s)] + G_d D(s) + EU(s) \tag{8.41}$$

Then, it is possible to obtain the desired plants from equation (8.41). To find the desired plants, it is required to disregard the input perturbation. So:

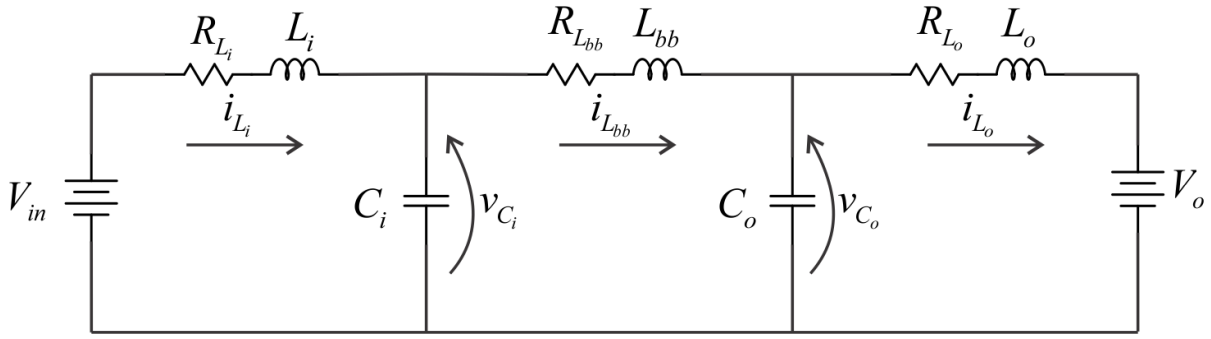
$$Y(s) = \left[C(Ks - A)^{-1}\right] \cdot [F_d D(s)] + G_d D(s) \tag{8.42}$$

$$\frac{Y(s)}{D(s)} = \left[C(Ks - A)^{-1}\right] \cdot F_d + G_d \tag{8.43}$$

8.4.2 Buck Dynamic Model

As the converter has five active elements, it is necessary to find five equations linearly independent in the model. According to Figure 8.13, is obtained:

Figure 8.13 – First topological state - Buck



Source: Own elaborated

$$-V_{in} + R_{L_i} i_{L_i} + L_i \frac{di_{L_i}}{dt} + v_{C_i} = 0 \tag{8.44}$$

$$-v_{C_i} + R_{L_{bb}} i_{L_{bb}} + L_{bb} \frac{di_{L_{bb}}}{dt} + v_{C_o} = 0 \tag{8.45}$$

$$-v_{C_o} + R_{L_o} i_{L_o} + L_o \frac{di_{L_o}}{dt} + V_o = 0 \tag{8.46}$$

$$C_i \frac{dv_{C_i}}{dt} = i_{L_i} - i_{L_{bb}} \tag{8.47}$$

$$C_i \frac{dv_{C_i}}{dt} = i_{L_i} - i_{L_{bb}} \tag{8.48}$$

From equations (8.44) to (8.48), it is possible to find the state space matrices on the form "$K_1 \cdot \dot{x} = A_1 \cdot x + B_1 \cdot u$". Then:

$$K_1 = \begin{bmatrix} L_i & 0 & 0 & 0 & 0 \\ 0 & L_{bb} & 0 & 0 & 0 \\ 0 & 0 & L_o & 0 & 0 \\ 0 & 0 & 0 & C_i & 0 \\ 0 & 0 & 0 & 0 & C_o \end{bmatrix} \tag{8.49}$$

$$A_1 = \begin{bmatrix} -R_{L_i} & 0 & 0 & -1 & 0 \\ 0 & -R_{L_{bb}} & 0 & 1 & -1 \\ 0 & 0 & -R_{L_o} & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \end{bmatrix} \tag{8.50}$$

$$B_1 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.51}$$

$$x = \begin{bmatrix} i_{L_i} \\ i_{L_o} \\ i_{L_{bb}} \\ v_{C_i} \\ v_{C_o} \end{bmatrix} \tag{8.52}$$

$$u = \begin{bmatrix} V_{in} \\ V_o \end{bmatrix} \tag{8.53}$$

For matrices $y = C \cdot x + E \cdot u$:

$$i_{in} = i_{L_{bb}} \tag{8.54}$$

$$i_o = i_{L_{bb}} \tag{8.55}$$

$$v_o = v_{C_o} \tag{8.56}$$

Hence:

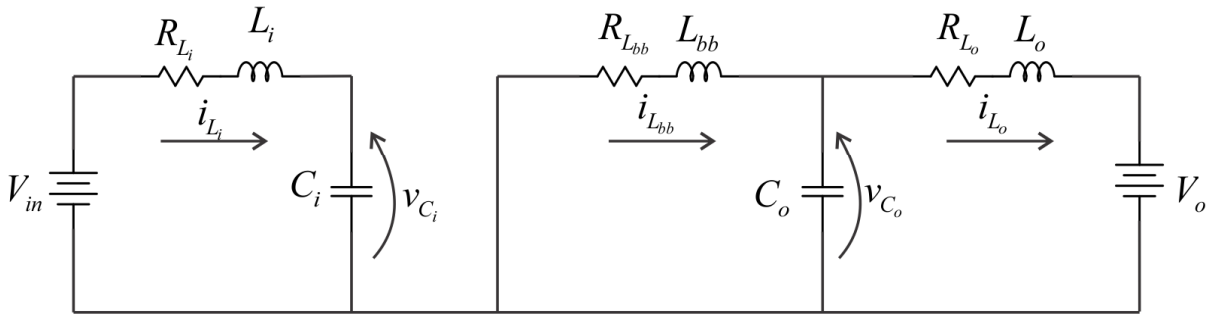
$$y = \begin{bmatrix} i_{in} \\ i_o \\ v_o \end{bmatrix} \tag{8.57}$$

$$C_1 = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{8.58}$$

$$E_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.59}$$

Similarly, it is necessary to find for the second topological state five equations that describe the circuit. Figure 8.14 presents the second topological state of Buck converter.

Figure 8.14 – Second topological state - Buck



Source: Own elaborated

$$-V_{in} + R_{L_i} i_{L_i} + L_i \frac{di_{L_i}}{dt} = 0 \tag{8.60}$$

$$R_{L_{bb}} i_{L_{bb}} + L_{bb} \frac{di_{L_{bb}}}{dt} + v_{C_o} = 0 \tag{8.61}$$

$$-v_{C_o} + R_{L_o} i_{L_o} + L_o \frac{di_{L_o}}{dt} + V_o = 0 \tag{8.62}$$

$$C_i \frac{dv_{C_i}}{dt} = i_{L_i} \tag{8.63}$$

$$C_o \frac{dv_{C_o}}{dt} = i_{L_{bb}} - i_{L_S} \tag{8.64}$$

From same equations (8.60) to (8.61), the state space matrices are defined:

$$K_2 = \begin{bmatrix} L_i & 0 & 0 & 0 & 0 \\ 0 & L_{bb} & 0 & 0 & 0 \\ 0 & 0 & L_o & 0 & 0 \\ 0 & 0 & 0 & C_i & 0 \\ 0 & 0 & 0 & 0 & C_o \end{bmatrix} \tag{8.65}$$

$$A_2 = \begin{bmatrix} -R_{L_i} & 0 & 0 & -1 & 0 \\ 0 & -R_{L_{bb}} & 0 & 0 & -1 \\ 0 & 0 & -R_{L_o} & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \end{bmatrix} \tag{8.66}$$

$$B_2 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.67}$$

And for the output, it is found the following equations:

$$i_{in} = 0 \tag{8.68}$$

$$i_o = i_{L_{bb}} \tag{8.69}$$

$$v_o = v_{C_o} \tag{8.70}$$

Hence:

$$y = \begin{bmatrix} i_{in} \\ i_o \\ v_o \end{bmatrix} \tag{8.71}$$

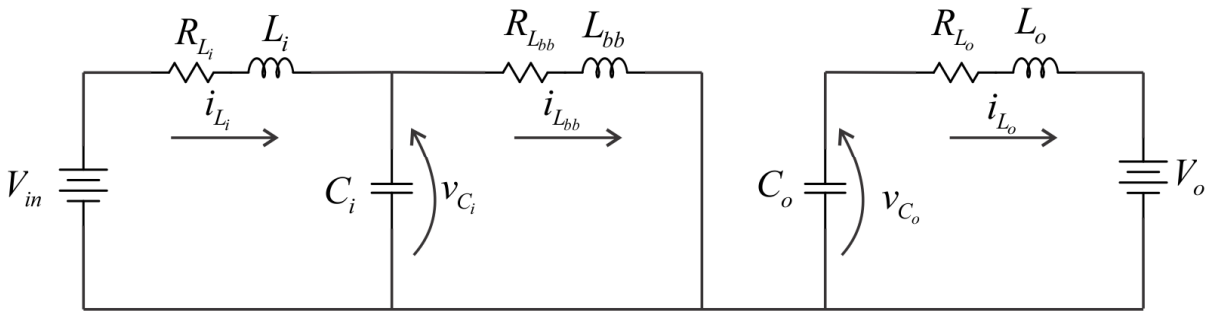
$$C_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{8.72}$$

$$E_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.73}$$

8.4.3 Boost Dynamic Model

Like the Buck dynamic model, the five equations for Boost model can be obtained from Figure 8.15.

Figure 8.15 – First topological state - Boost



Source: Own elaborated

$$-V_{in} + R_{L_i} i_{L_i} + L_i \frac{di_{L_i}}{dt} + v_{C_i} = 0 \tag{8.74}$$

$$-v_{C_i} + R_{L_{bb}} i_{L_{bb}} + L_{bb} \frac{di_{L_{bb}}}{dt} + v_{C_o} = 0 \tag{8.75}$$

$$-v_{C_o} + R_{L_o} i_{L_o} + L_o \frac{di_{L_o}}{dt} + V_o = 0 \tag{8.76}$$

$$C_i \frac{dv_{C_i}}{dt} = i_{L_i} - i_{L_{bb}} \tag{8.77}$$

$$C_o \frac{dv_{C_o}}{dt} = -i_{L_o} \tag{8.78}$$

$$K_1 = \begin{bmatrix} L_i & 0 & 0 & 0 & 0 \\ 0 & L_{bb} & 0 & 0 & 0 \\ 0 & 0 & L_o & 0 & 0 \\ 0 & 0 & 0 & C_i & 0 \\ 0 & 0 & 0 & 0 & C_o \end{bmatrix} \tag{8.79}$$

$$A_1 = \begin{bmatrix} -R_{L_i} & 0 & 0 & -1 & 0 \\ 0 & -R_{L_{bb}} & 0 & 1 & 0 \\ 0 & 0 & -R_{L_o} & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \tag{8.80}$$

$$B_1 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.81}$$

$$x = \begin{bmatrix} i_{L_i} \\ i_{L_o} \\ i_{L_{bb}} \\ v_{C_i} \\ v_{C_o} \end{bmatrix} \tag{8.82}$$

$$u = \begin{bmatrix} V_{in} \\ V_o \end{bmatrix} \tag{8.83}$$

For matrices $y = C \cdot x + E \cdot u$, the following equations are used:

$$i_{in} = i_{L_{bb}} \tag{8.84}$$

$$i_o = 0 \tag{8.85}$$

$$v_o = v_{C_o} \tag{8.86}$$

Hence:

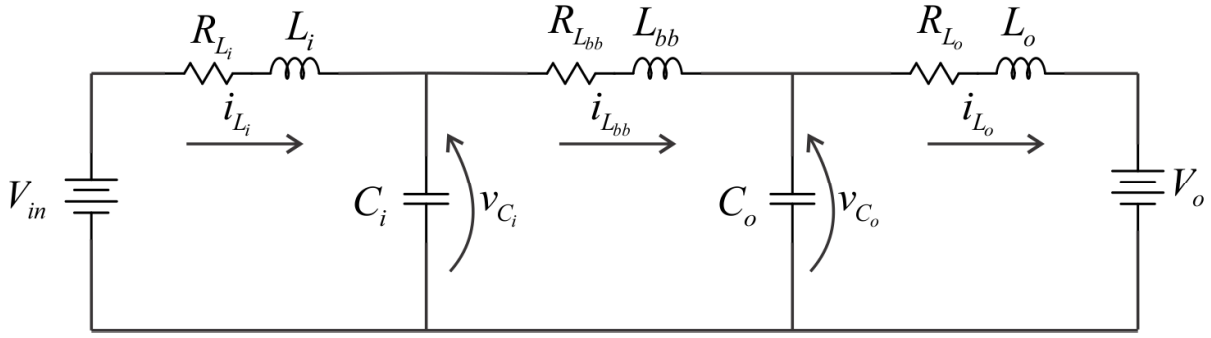
$$y = \begin{bmatrix} i_{in} \\ i_o \\ v_o \end{bmatrix} \tag{8.87}$$

$$C_1 = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{8.88}$$

$$E_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.89}$$

For second topological state, the five equations are extracted from Figure 8.16 analysis.

Figure 8.16 – Second topological state - Boost



Source: Own elaborated

$$-V_{in} + R_{L_i} i_{L_i} + L_i \frac{di_{L_i}}{dt} + v_{C_i} = 0 \tag{8.90}$$

$$-v_{C_i} + R_{L_{bb}} i_{L_{bb}} + L_{bb} \frac{di_{L_{bb}}}{dt} + v_{C_o} = 0 \tag{8.91}$$

$$-v_{C_o} + R_{L_o} i_{L_o} + L_o \frac{di_{L_o}}{dt} + V_o = 0 \tag{8.92}$$

$$C_i \frac{dv_{C_i}}{dt} = i_{L_i} - i_{L_{bb}} \tag{8.93}$$

$$C_o \frac{dv_{C_o}}{dt} = i_{L_{bb}} - i_{L_S} \tag{8.94}$$

$$K_2 = \begin{bmatrix} L_i & 0 & 0 & 0 & 0 \\ 0 & L_{bb} & 0 & 0 & 0 \\ 0 & 0 & L_o & 0 & 0 \\ 0 & 0 & 0 & C_i & 0 \\ 0 & 0 & 0 & 0 & C_o \end{bmatrix} \tag{8.95}$$

$$A_2 = \begin{bmatrix} -R_{L_i} & 0 & 0 & -1 & 0 \\ 0 & -R_{L_{bb}} & 0 & 1 & -1 \\ 0 & 0 & -R_{L_o} & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \end{bmatrix} \tag{8.96}$$

$$B_2 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.97}$$

$$x = \begin{bmatrix} i_{L_i} \\ i_{L_o} \\ i_{L_{bb}} \\ v_{C_i} \\ v_{C_o} \end{bmatrix} \tag{8.98}$$

$$u = \begin{bmatrix} V_{in} \\ V_o \end{bmatrix} \tag{8.99}$$

For matrices $y = C \cdot x + E \cdot u$:

$$i_{in} = i_{L_{bb}} \tag{8.100}$$

$$i_o = i_{L_{bb}} \tag{8.101}$$

$$v_o = v_{C_o} \tag{8.102}$$

Hence:

$$y = \begin{bmatrix} i_{in} \\ i_o \\ v_o \end{bmatrix} \tag{8.103}$$

$$C_2 = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{8.104}$$

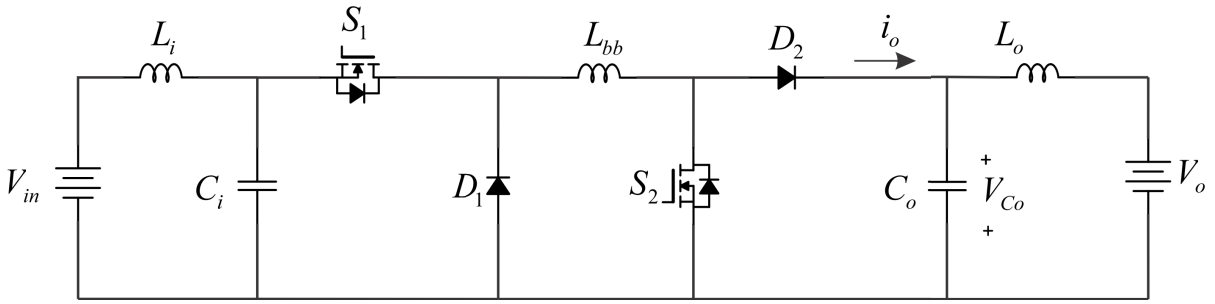
$$E_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{8.105}$$

8.5 CONVERTER NUMERICAL PLANTS AND COMPENSATOR DESIGN

The algebraic plants found in the previous subsection resulted in a very large sum of partial fractions, which is difficult to simplify even computer-aided. Then, knowing the values of inductances, capacitances, and resistances of the converter, it is possible to obtain the numerical values of the plant. Figure 8.17 shows the model used to find the output current and the voltage response for a step in the duty cycle. The output current is measured on the diode D_2 and the output voltage on the capacitor C_o.

Also it was added the series resistance in each inductor in order to obtain a inverse state matrix. The resistances used were a very low arbitrary value, wherein their inclusion has no considerable effect on the plants.

Figure 8.17 – Converter Structure for Control Plant



Source: Own elaborated

For Buck mode:

$$V_{in} = 730V \tag{8.106}$$
$$V_o = 526V \tag{8.107}$$
$$C_i = 7.2mF \tag{8.108}$$
$$Li = 1nH \tag{8.109}$$
$$L_{bb} = 450\mu H \tag{8.110}$$
$$C_o = 7.2mF \tag{8.111}$$
$$L_o = 1nH \tag{8.112}$$
$$R_{L_{bb}} = 1m\Omega \tag{8.113}$$
$$R_{L_i} = 1m\Omega \tag{8.114}$$
$$R_{L_o} = 1m\Omega \tag{8.115}$$

Then, using equations of the state-space model, and the matrices found in Buck Dynamic Model Section, the plants are:

$$G_{Vco_d_buck}(s) = \frac{V_{co}(s)}{d(s)} = \frac{4.5062 \cdot 10^8 \left(s + 10^6\right)}{(s + 5.598)\left(s^2 + 10^6 s + 2.778 \cdot 10^{11}\right)} \tag{8.116}$$

$$G_{Io_d_buck}(s) = \frac{I_{out}(s)}{d(s)} = \frac{1.622 \cdot 10^6}{s + 5.598} \tag{8.117}$$

For Boost mode:

$$V_{in} = 526V \tag{8.118}$$
$$V_o = 730V \tag{8.119}$$
$$C_i = 7.2mF \tag{8.120}$$
$$Li = 1nH \tag{8.121}$$
$$L_{bb} = 450\mu H \tag{8.122}$$
$$C_o = 7.2mF \tag{8.123}$$
$$L_o = 1nH \tag{8.124}$$
$$R_{L_{bb}} = 1m\Omega \tag{8.125}$$
$$R_{L_i} = 1m\Omega \tag{8.126}$$
$$R_{L_o} = 1m\Omega \tag{8.127}$$

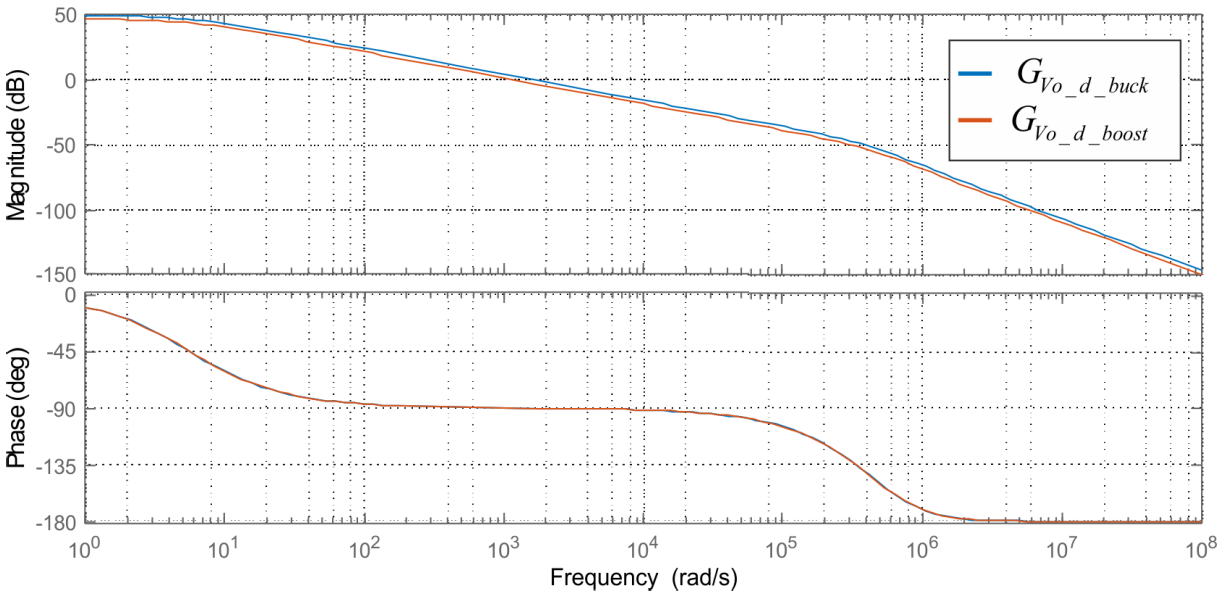
As with the Buck, using equations of the state-space model, and the matrices found in Boost Dynamic Model Section, the plants are:

$$G_{Vco_d_boost}(s) = \frac{V_{co}(s)}{d(s)} = \frac{\begin{array}{l}1.0895 \cdot 10^{-8}\left(s + 2.98 \cdot 10^{16}\right)\\ \left(s + 10^{6}\right)\left(s^2 + 10^{6}s + 2.771 \cdot 10^{11}\right)\\ \left(s^2 + 9.954 \cdot 10^{5}s + 2.759 \cdot 10^{11}\right)\\ \left(s^2 + 1.004 \cdot 10^{6}s + 2.804 \cdot 10^{11}\right)\end{array}}{\left(s + 5.598\right)\left(s^2 + 10^{6}s + 2.778 \cdot 10^{11}\right)^4} \tag{8.128}$$

$$G_{Io_d_boost}(s) = \frac{I_{out}(s)}{d(s)} = \frac{\begin{array}{l}3.9222 \cdot 10^{-11}\left(s + 2.98 \cdot 10^{16}\right)\\ \left(s^2 + 1.01 \cdot 10^{6}s + 2.785 \cdot 10^{11}\right)\\ \left(s^2 + 9.736 \cdot 10^{5}s + 2.633 \cdot 10^{11}\right)\\ \left(s^2 + 1.026 \cdot 10^{6}s + 2.93 \cdot 10^{11}\right)\\ \left(s^2 + 9.9 \cdot 10^{5}s + 2.772 \cdot 10^{11}\right)\end{array}}{\left(s + 5.598\right)\left(s^2 + 10^{6}s + 2.778 \cdot 10^{11}\right)^4} \tag{8.129}$$

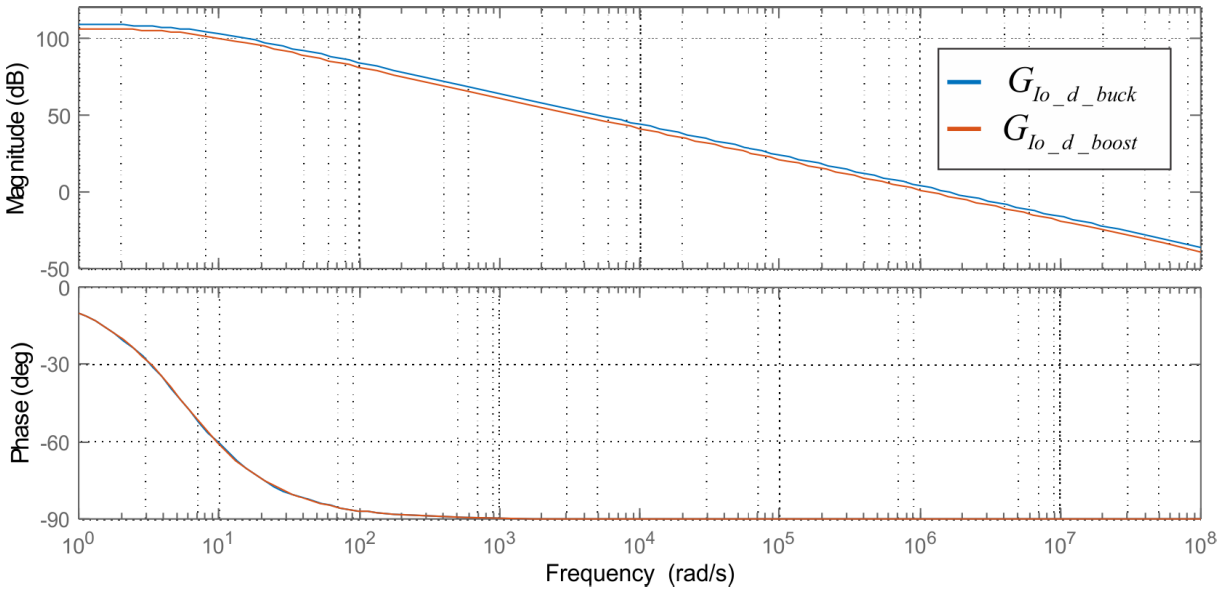
Figures 8.18 and 8.19 show the Bode diagram of the transfer function for the duty cycle step response concerning to output current and output voltage, respectively. The graphs show that the plants for Buck and Boost are very similar, which allows designing a suitable compensator for both the operation mode of the converter.

Figure 8.18 – Bode Diagram - Output Voltage



Source: Own elaborated

Figure 8.19 – Bode Diagram - Output Current

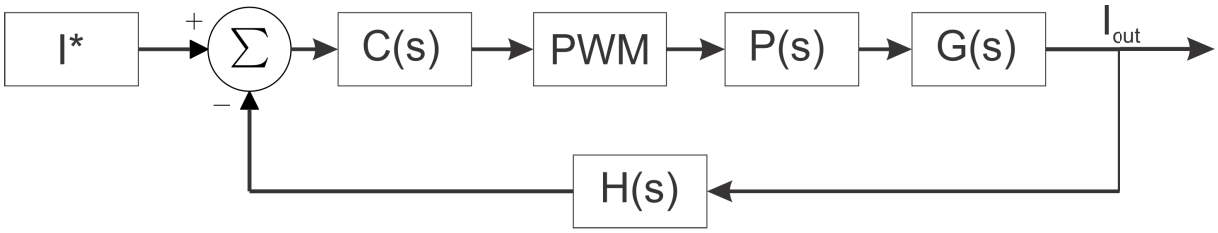


Source: Own elaborated

The designed compensator was based on the current plant for two reasons. Firstly, in the Boost mode, the dynamics of the current are higher than the voltage, even for resistive loads; and the current has an impact on the voltage control, due to droop control method. The other reason is that in battery operation the output voltage is already defined. So, any change in the dynamics will be impacted by the current.

Figure 8.20 presents the block diagram of the control strategy.

Figure 8.20 – Block Diagram



Source: Own elaborated

Wherein:

- I^* is the current reference;
- $C(s)$ is the compensator;
- PWM is the modulator gain;
- $P(s)$ is the Pade Approximation;
- $G(s)$ is the plant;
- $H(s)$ is measurement gain, including the filters;
- I_{out} is the output current.

The PWM is the gain of the carrier signal. In the microcontroller used, to achieve a 20 kHz switching signal, the PWM gain is:

$$PWM = \frac{1}{4500} \tag{8.130}$$

The Pade Approximation is a technique used to compensate for the delay when the microcontroller is updating the duty cycle. In other words, during a switching period, the microcontroller will be calculating the next duty cycle, which differs from analogical compensators. In that case, the Pade Approximation is:

$$P(s) = \frac{20000 - 0.75 \cdot s}{20000 + 0.75 \cdot s} \tag{8.131}$$

The $H(s)$ is the gain of the sensors. For current and voltage, the gains were compensated internally by the microprocessor. But as there were two low pass filters in cascade for each sensor, this impacted the dynamic of measuring the values. It is formed by two RC circuits presented on Annex C, which lead to a transfer function of:

$$H(s) = \frac{62500000000}{(121s + 250000)^2} \tag{8.132}$$

Then, the non-compensated open-loop transfer function is defined as:

$$OLTF_{NC}(s) = G(s) \cdot P(s) \cdot H(s) \cdot PWM \tag{8.133}$$

A Proportional-Integral (PI) was selected to provide null error to step response. To calculate the compensator, it was chosen the Boost plant, once its output current is pulsed and the control needs to be carefully designed. Then:

$$OLTF_{NC}(s) = G_{Vco_d_boost}(s) \cdot P(s) \cdot H(s) \cdot PWM \tag{8.134}$$

The cutoff frequency chosen was three decades behind the switching frequency, which a phase margin of 60 degrees.

$$\omega_c = \frac{2\pi \cdot 20000}{1000} = 125.664(rad/s) \tag{8.135}$$

$$M_f = 60^o \tag{8.136}$$

Then:

$$\omega_z = \frac{\omega_c}{\tan(M_f - 45 - \arg(OPTF_{NC}(\omega_c))} \tag{8.137}$$

$$\omega_z = 68.312 \tag{8.138}$$

And:

$$k_c = \frac{\omega_c}{\sqrt{\omega_z^2 + \omega_c^2} \cdot |OPTF_{NC}(\omega_c)|} \tag{8.139}$$

$$k_c = 0.213 \tag{8.140}$$

Then, the compensator is calculated as:

$$C(s) = \frac{k_c(s + \omega_z)}{s} \tag{8.141}$$

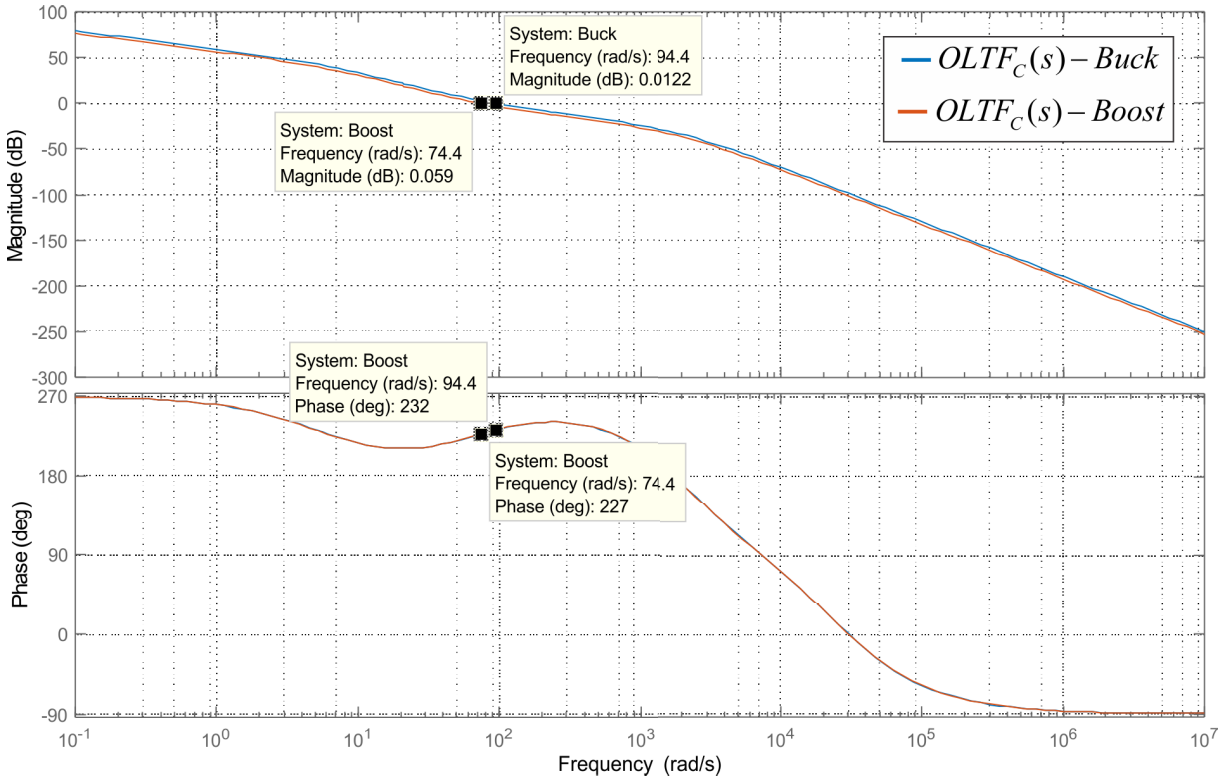
$$C(s) = \frac{0.213s + 14.55}{s} \tag{8.142}$$

The open-loop compensated transfer function is:

$$OLTF_C(s) = C(s) \cdot OPTF_{NC}(s) \tag{8.143}$$

The Bode graph for the transfer function shown in equation (8.143) is presented on Figure 8.21. Also, it is plotted the open-loop compensated transfer function for Buck mode, with the same compensator calculated for Boost.

Figure 8.21 – Compensated Open Loop Transfer Functions - Output Current



Source: Own elaborated

Figure (8.143) shows that the compensated transfer function has a very close dynamic, which allows operating the converter with stability in both operation modes.

The compensator now needs to be translated to be digitally implemented. Then, it is used the Tustin discretization:

$$C(z) = \frac{0.2133637614 - 0.2126362386 \cdot z^{-1}}{1 - z^{-1}} \tag{8.144}$$

It is also known that the compensator is:

$$C(z) = \frac{duty(z)}{error(z)} \tag{8.145}$$

Transforming the discrete transfer function to a difference discrete equation:

$$duty(n) = duty(n-1) + 0.2133637614 \cdot error(n) - 0.2126362386 \cdot error(n-1) \tag{8.146}$$

The equation (8.146) is used in the microprocessor to perform the control. Once found this equation, it is possible to implement the control strategy proposed in Figure 8.12.

8.6 PARTIAL CONCLUSIONS

This chapter addresses the droop control technique which allows the current sharing of interconnected converters, avoiding the use of communication. Basically, the strategy is setting a static converter as a voltage controlled source and with an output resistance. Then, each converter will interact among themselves to find the balance point that defines the output voltage.

Then, the virtual resistances are introduced to the system to avoid the use of physical resistors. It can be achieved with the interaction of the control strategy that measures the current to define the voltage reference.

After, it is presented the state-space modeling of the converter using matrices. So, the plants are presented and it is designed the compensator. Although the numerical solution seems difficult to calculate manually, it can be easily calculated and designed when computer-aided.

Once projected the converter and also defined its control method, the implementation can be done to validate the theory presented.

9 EXPERIMENTAL RESULTS

From the above mathematical development and hardware design, the charging technique can be evaluated and tested. In the first moment, it is verified the converter operation. After, the droop control is implemented and the theory is checkout with practice.

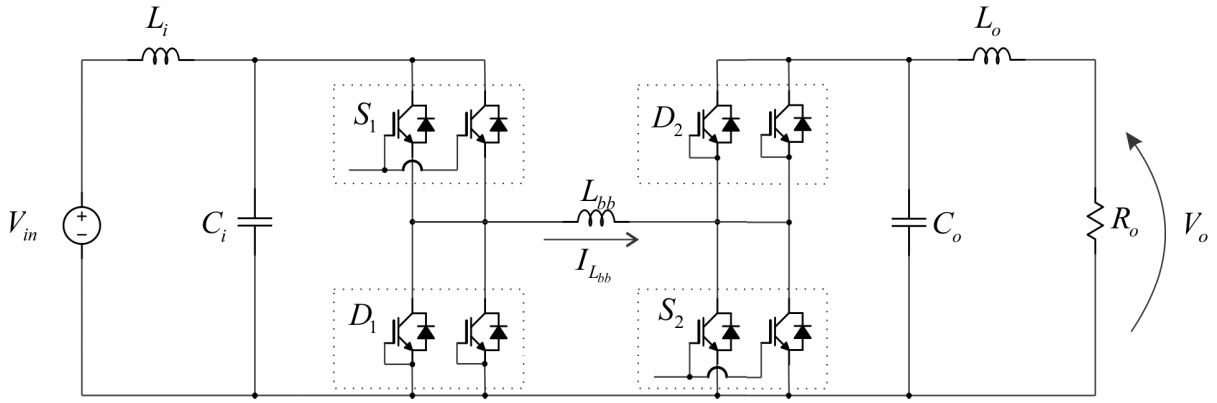
9.1 OPEN LOOP OPERATION

With the converter built, the voltage waveforms on Gate, IGBT, and diode were verified to know if the converter can be safely controlled on its operation region.

9.1.1 Buck Operation

In Buck operation, it was connected to a resistive load on the output. The duty cycle was controlled manually. Figure 9.1 presents the layout diagram of the test. To test the Buck circuit, the gate of $S2$ was configured to be always in a low state, while applied a constant duty cycle at $S1$ gate.

Figure 9.1 – Open Loop Test Setup



Source: Own elaborated

The tests were limited to the laboratory infrastructure, which only allows extraction of 15 kW, limited by the CC voltage source. To obtain open-loop results, the parameters used on the configuration were:

- V_{in} = 750 V
- duty cycle = 0.71
- R_o = 21.9 Ω

In this combination, the converter is operating in Continuous Conduction Mode, in which it was designed for. Thereby, the duty cycle will set the output voltage to:

$$V_o = V_{in} \cdot D \tag{9.1}$$

$$V_o = 532.5V \tag{9.2}$$

Figures 9.2 to 9.7 presents the waveforms taken from this operation.

Figure 9.2 – V_{S1} and Gate Voltage (Gate turn on)

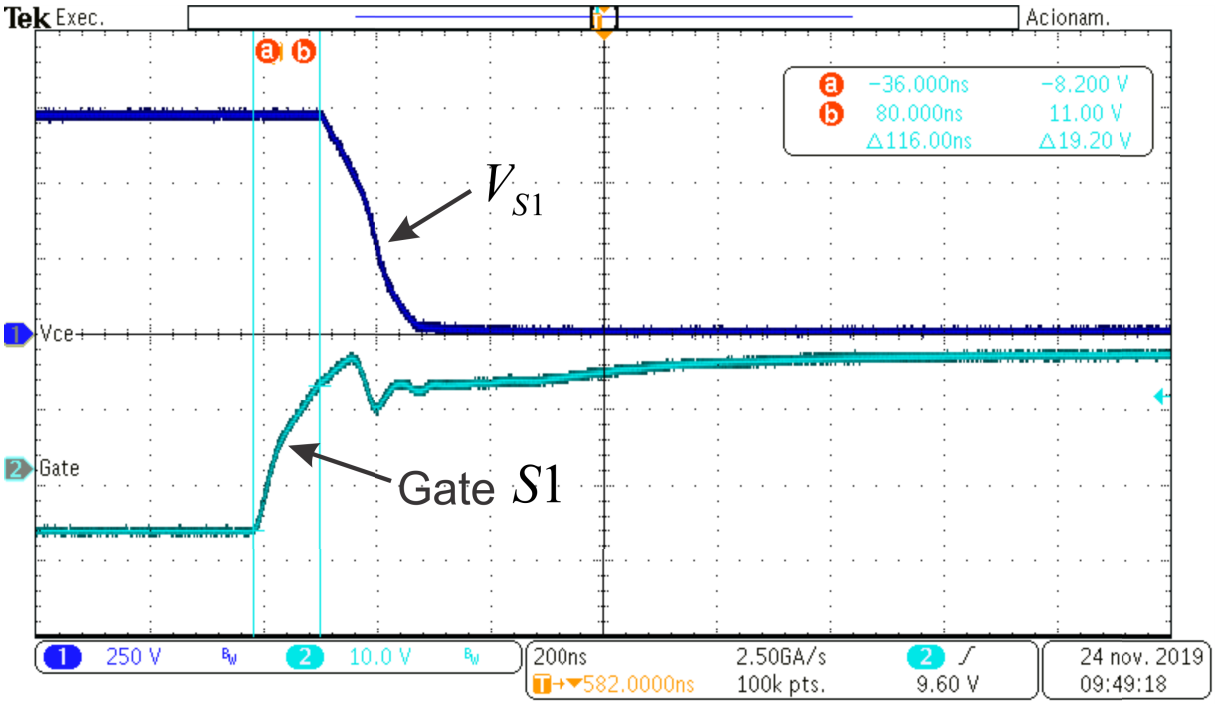


Figure 9.3 – V_{S1} and Gate Voltage (Gate turn off)

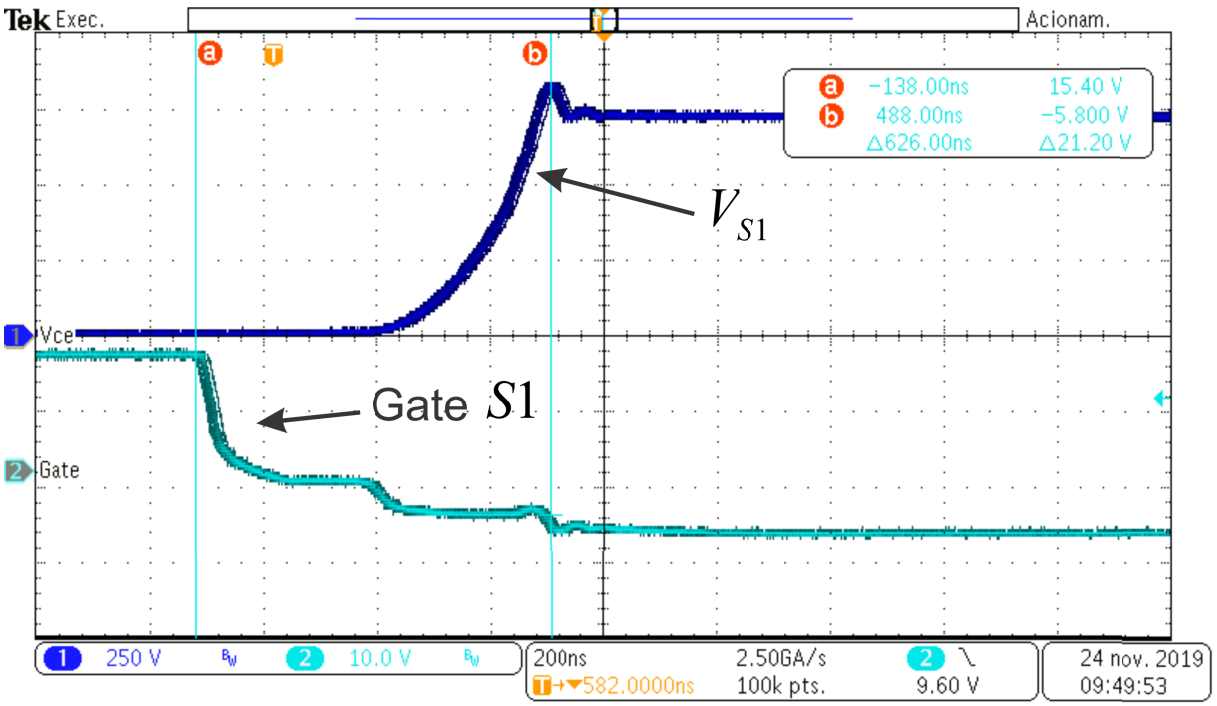


Figure 9.4 – V_{S1} and V_{D1} - Transition Gate OFF to Gate ON

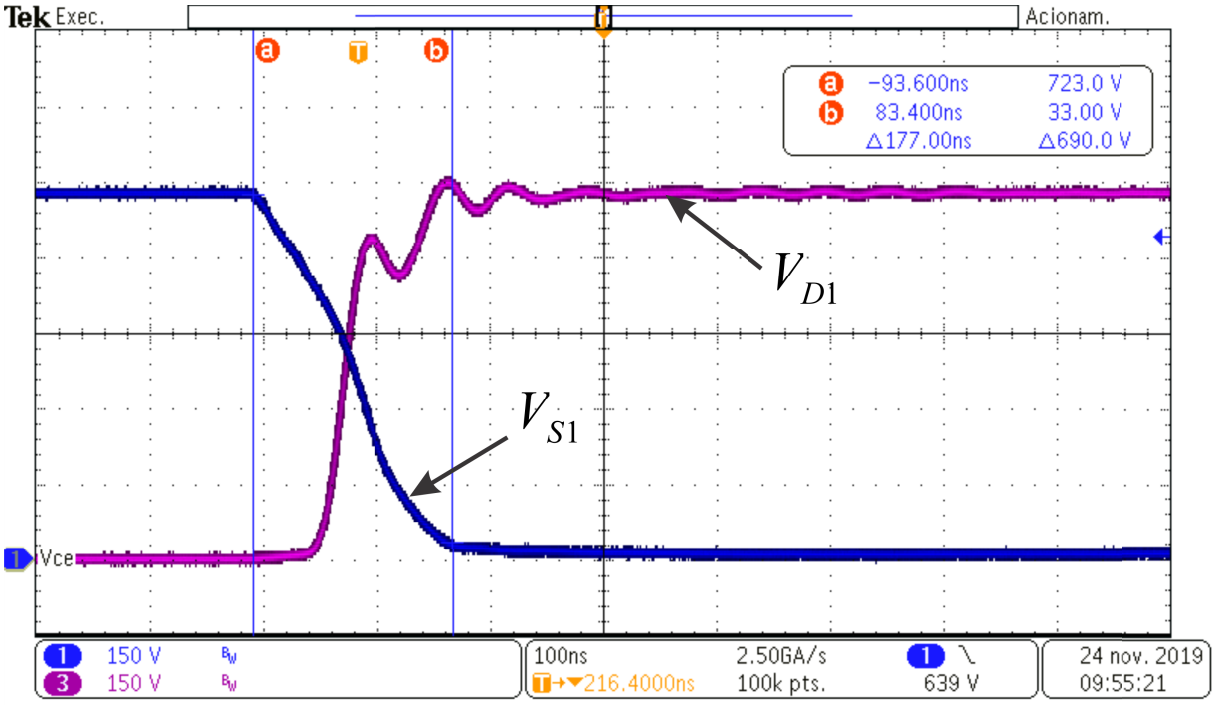


Figure 9.5 – V_{S1} and V_{D1} - Transition Gate ON to Gate OFF

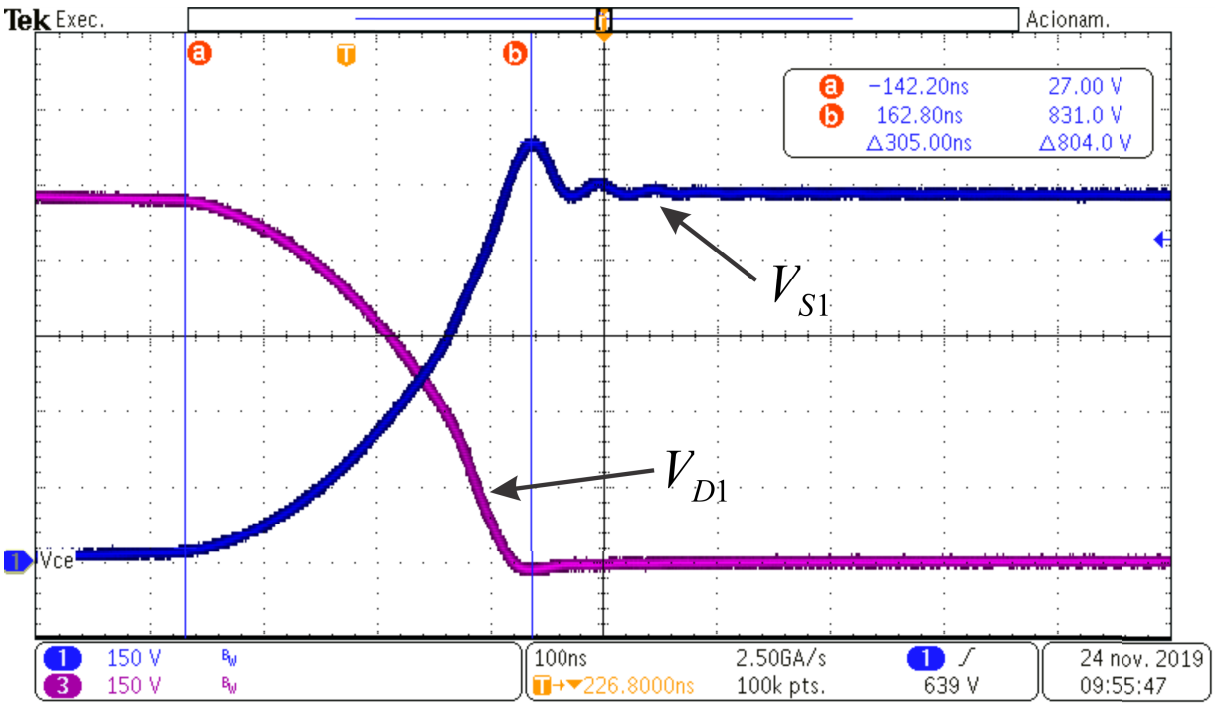


Figure 9.6 – V_{S1} and $I_{L_{bb}}$

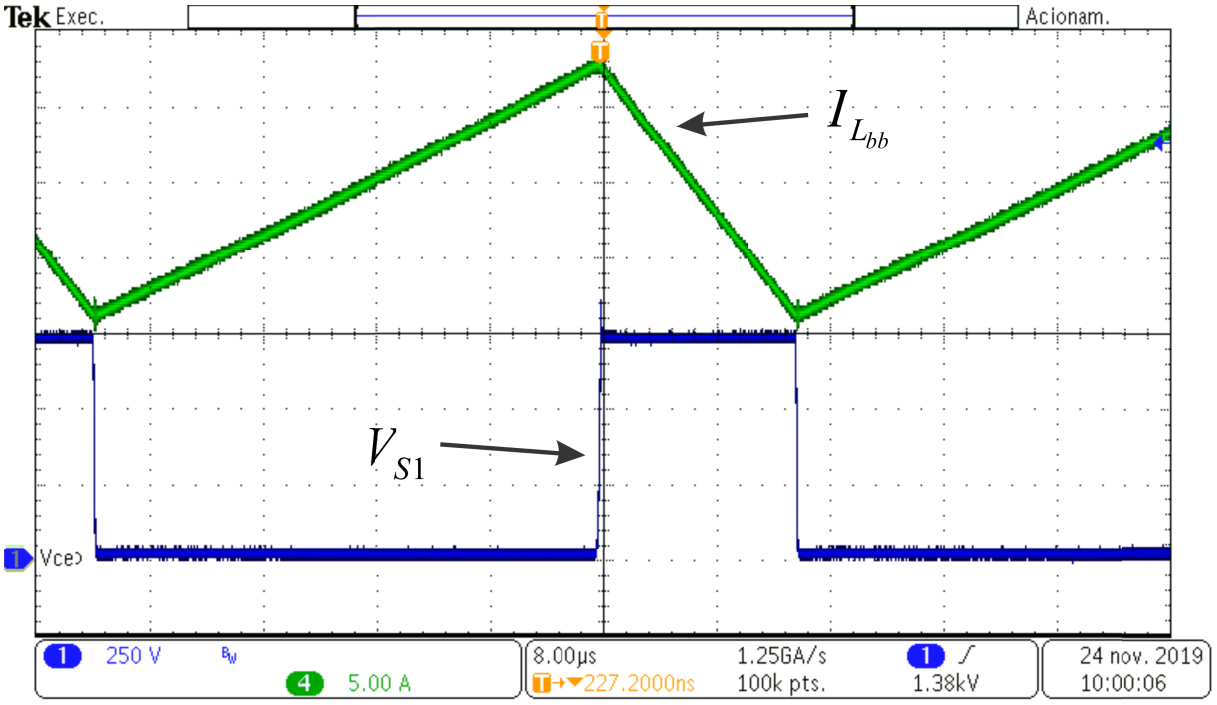
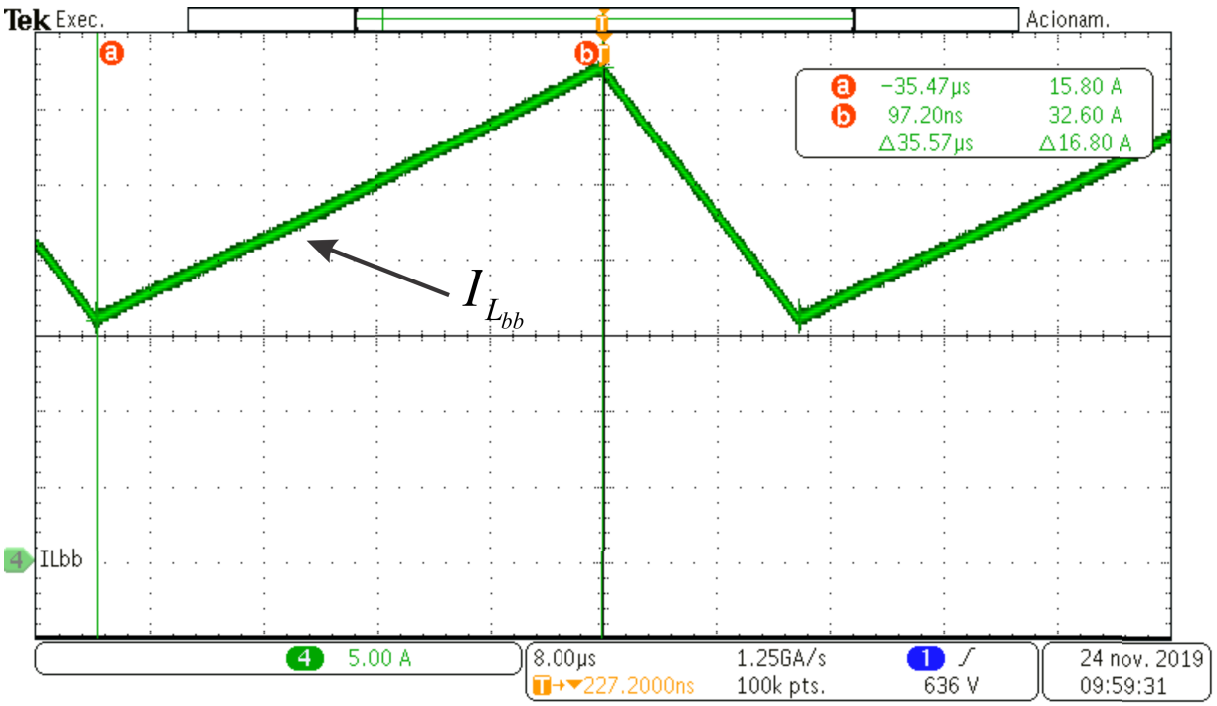


Figure 9.7 – $I_{L_{bb}}$ Ripple



9.1.2 Boost Operation

Similarly to Buck operation, the Boost was connected to a resistive load on the output and manually controlled the duty cycle. Figure 9.1 presents the layout diagram of the test. For the Boost, the $S1$ gate was configured to be always at a high state, and at $S2$ it was applied a constant duty cycle.

- V_{in} = 530 V
- duty cycle = 0.29
- R_o = 24.8 Ω

The output resistor has been chosen to the converter operates in CCM. Figures 9.8 to 9.13 presents the waveforms taken from this operation.

Figure 9.8 – V_{S2} and Gate Voltage (Gate turn on)

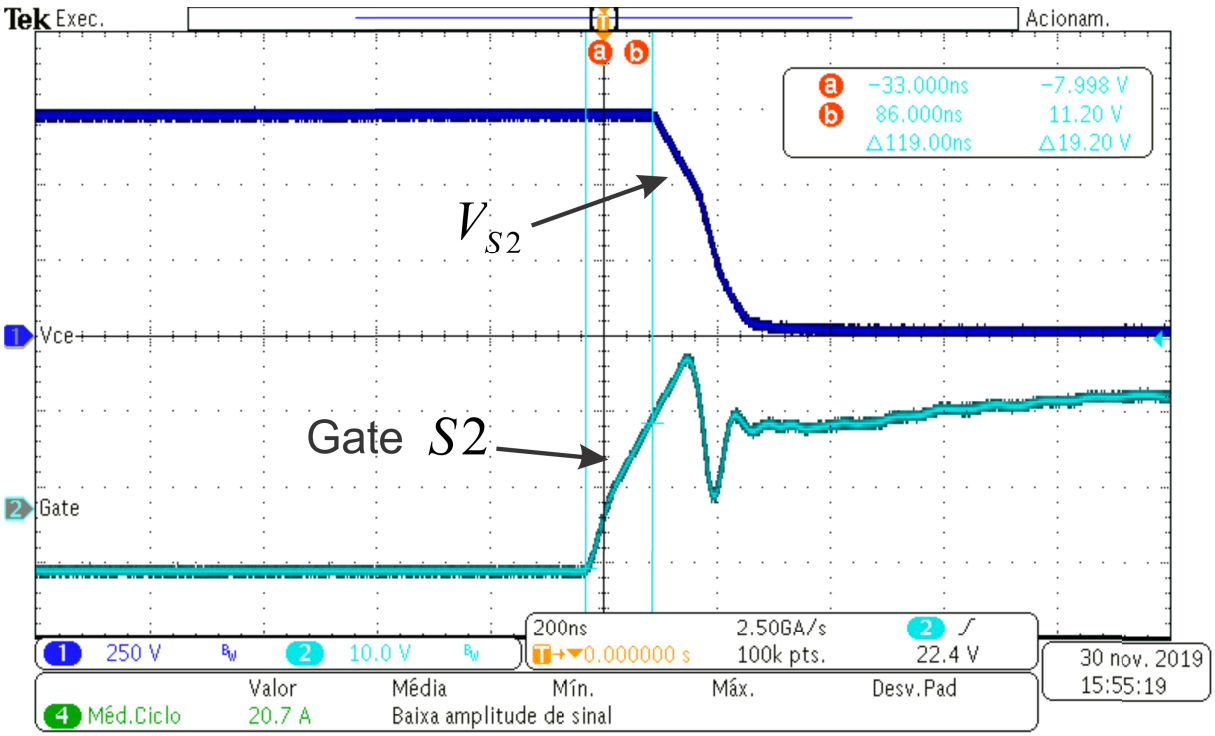


Figure 9.9 – V_{S2} and Gate Voltage (Gate turn off)

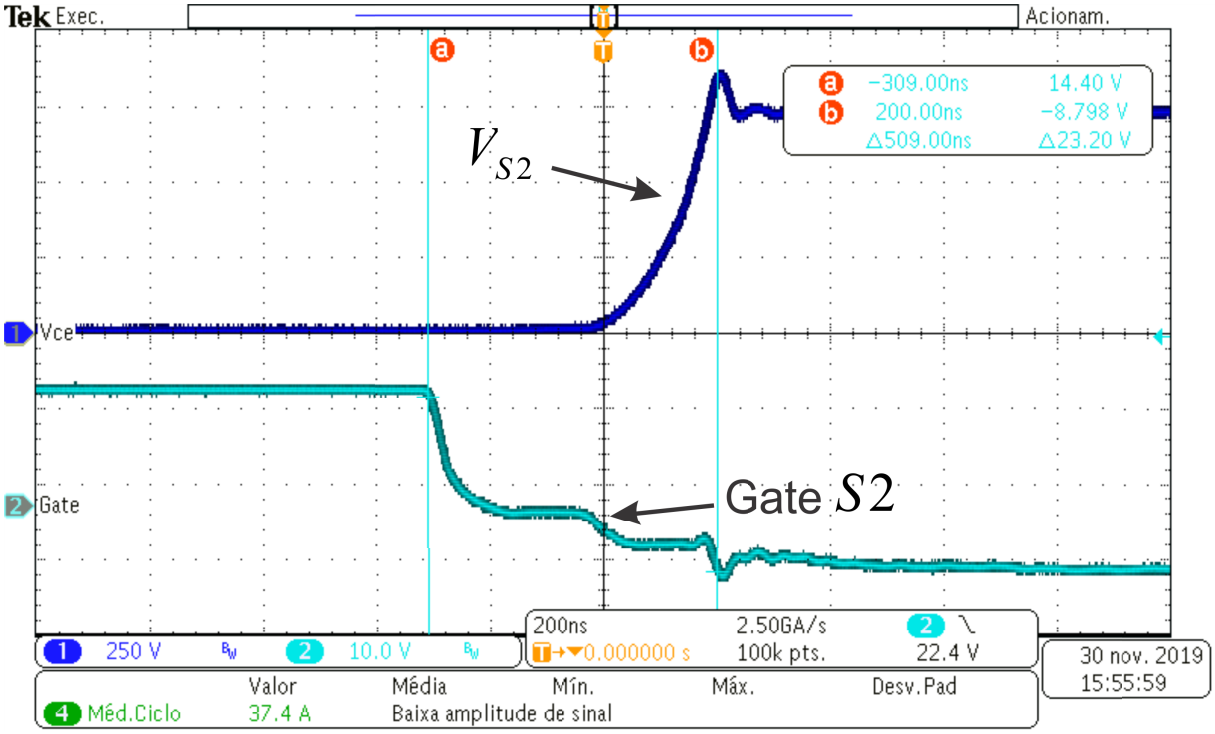


Figure 9.10 – V_{S2} and V_{D2} - Transition Gate OFF to Gate ON

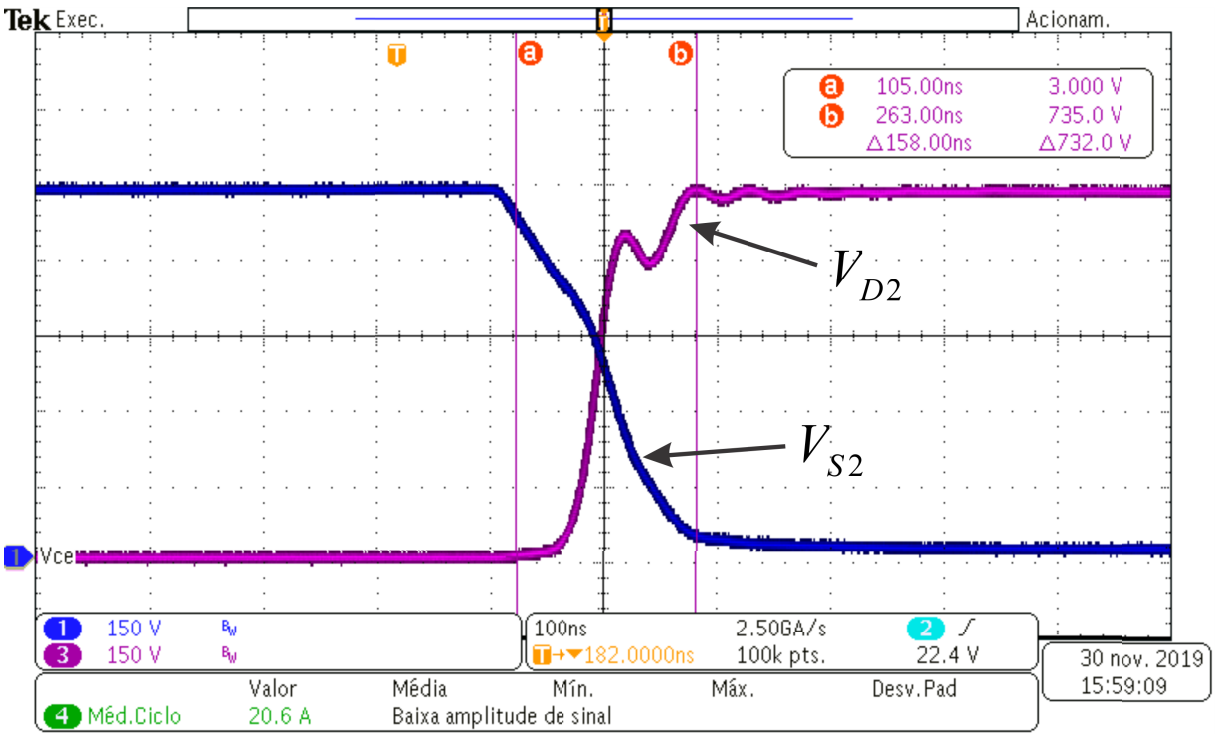


Figure 9.11 – V_{S2} and V_{D2} - Transition Gate ON to Gate OFF

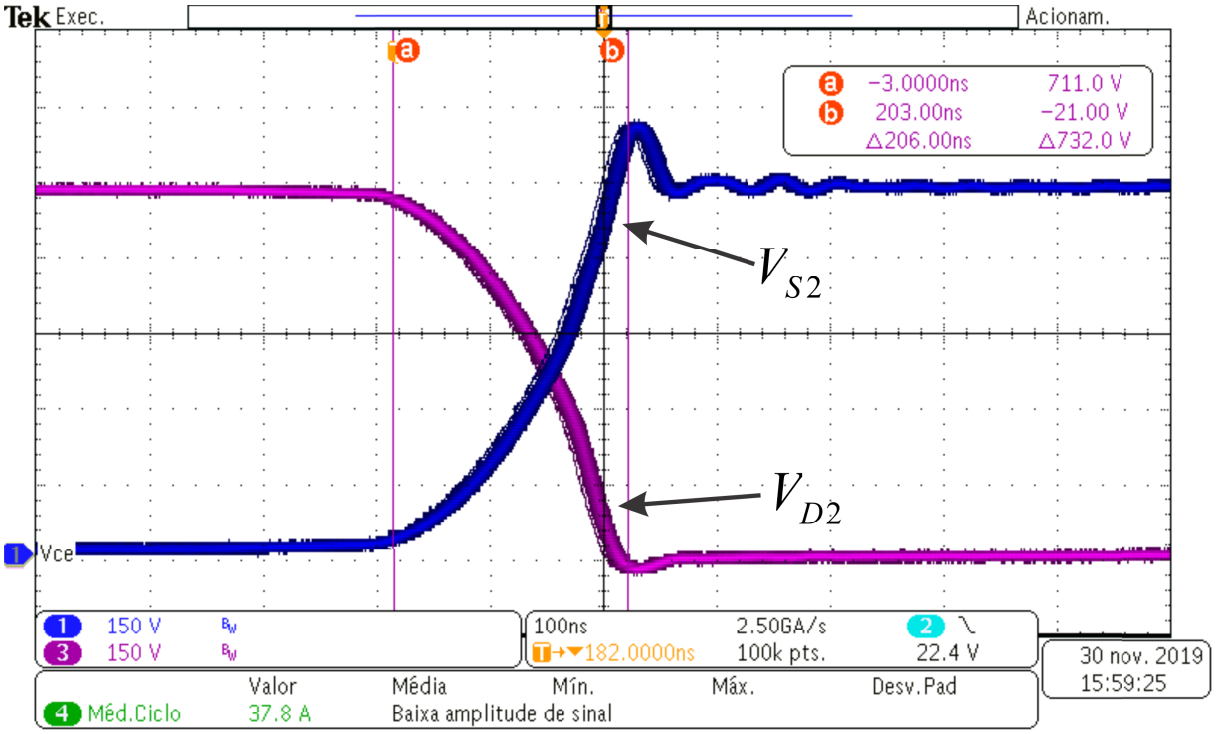


Figure 9.12 – V_{S2} and $I_{L_{bb}}$

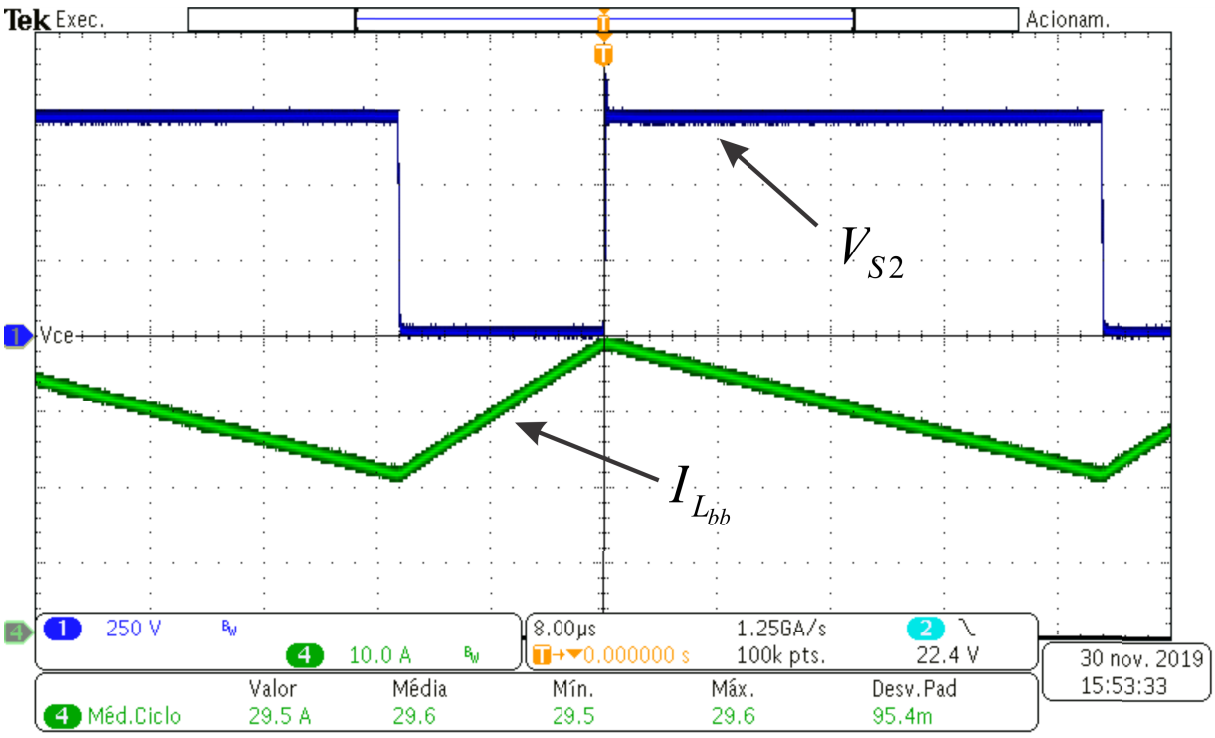
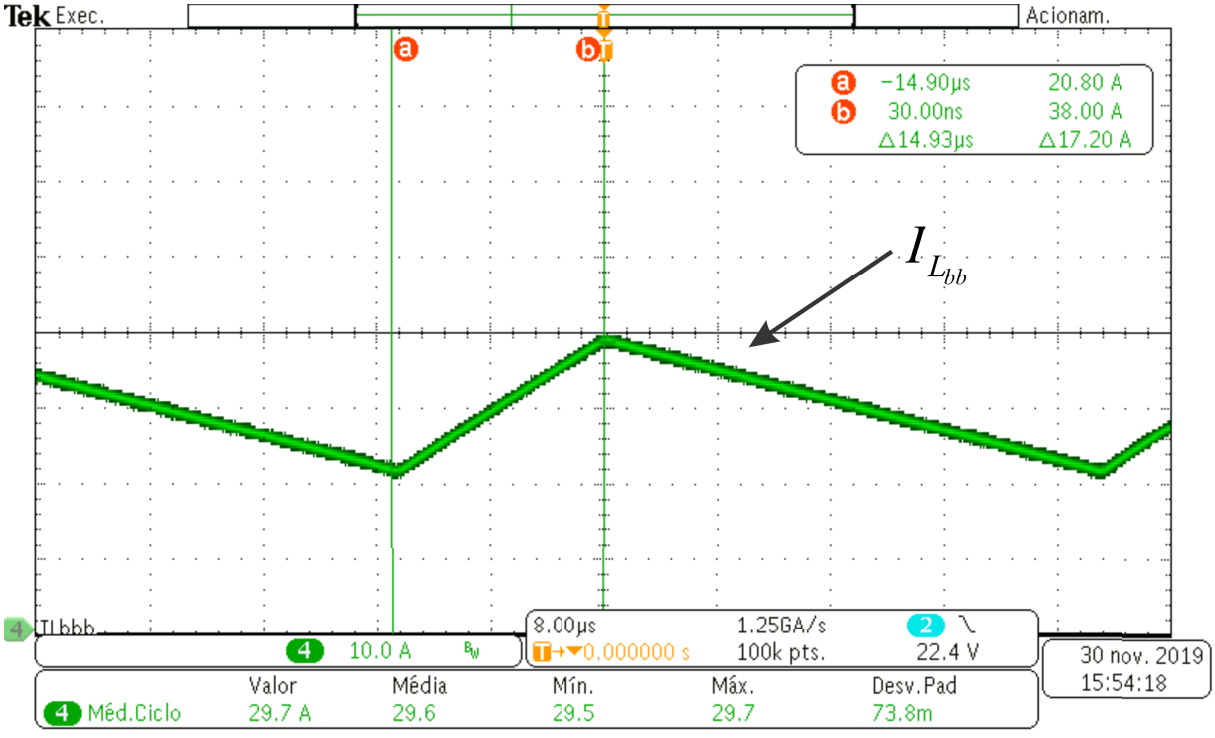


Figure 9.13 – $I_{L_{bb}}$ Ripple



9.1.3 Open Loop Results

The objective for testing the converter in open-loop was to check its performance and to verify if there is a necessity of adjustment of electronic parameters, such as gate resistors or Snubber circuits.

Then, no modification to the circuit parameters was needed to achieve those waveforms. However, several adjustments on the ground circuit were required, as well as the improvement of cabling connections among the printed circuit boards of the converter.

Those modifications were required due to the EMI noise created by the cooper bars on the converter, which was interfering with the gating signals. When a gate circuit was toggle from low to a high state, it could be observed a sudden drop on its voltage, as seen on Figures 9.2 and 9.8. The improvement of cabling reduced this effect. Also, the gate measurements could have been affected by the scope probes connected.

So, once performed the improvements, the voltage overshoots were harmful to the converter, as the IGBTs and diodes were rated 1200 V.

The ripple on the inductors from Figures 9.7 and 9.13 can be compared to the equations (5.7) and (6.7), which define the ripple current given the parameters. The results were presented in Table 9.1.

Table 9.1 – Inductor Verification

Operation	**Experimental Ripple Current (A)**	**Theorical Ripple Current (A)**	**Error**
Buck	16.8	17.16	2.09%
Boost	17.2	17.07	0.78%

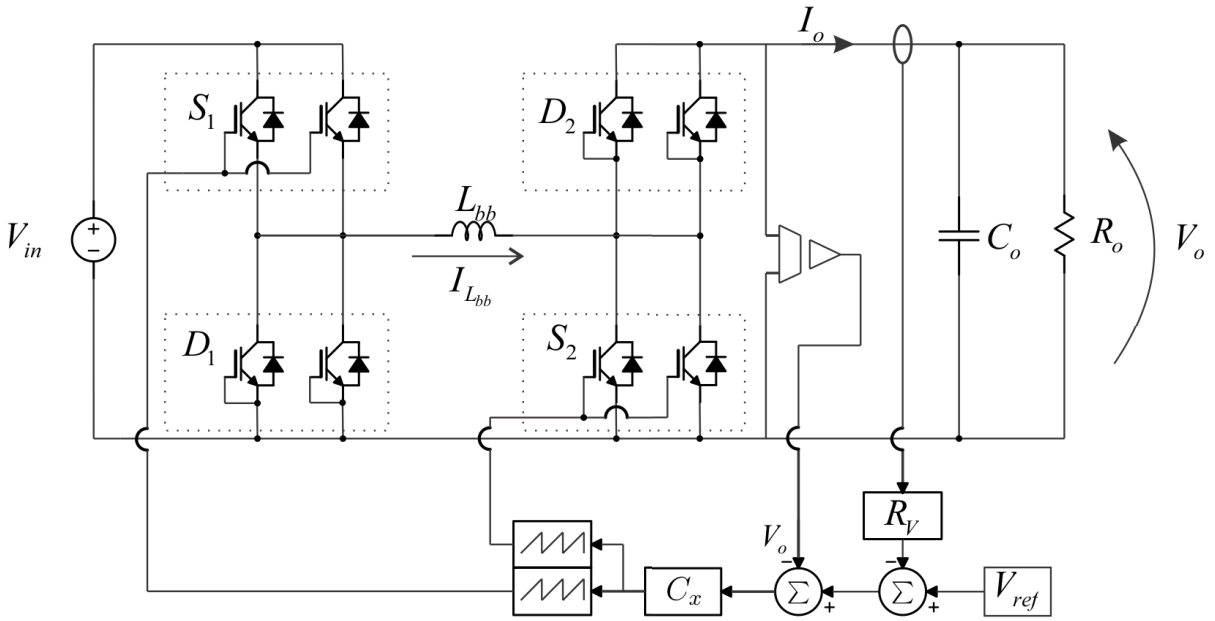
Source: Own Elaborated

Table 9.1 shows that the greatest error found was near two percent. Due to the precision of the measurement equipment and the inductance variation (manufacturing process), this error is acceptable.

9.2 VIRTUAL RESISTANCES

After both converters working properly, the virtual resistances technique was implemented. The digital control was applied with the feedback sensors, allowing the configuration of the virtual resistances. With a single converter operating, a setup with multiple combinations of output load was mounted to verify the V_o versus I_o, presented in Figure 9.14.

Figure 9.14 – Test Setup - Virtual Resistances



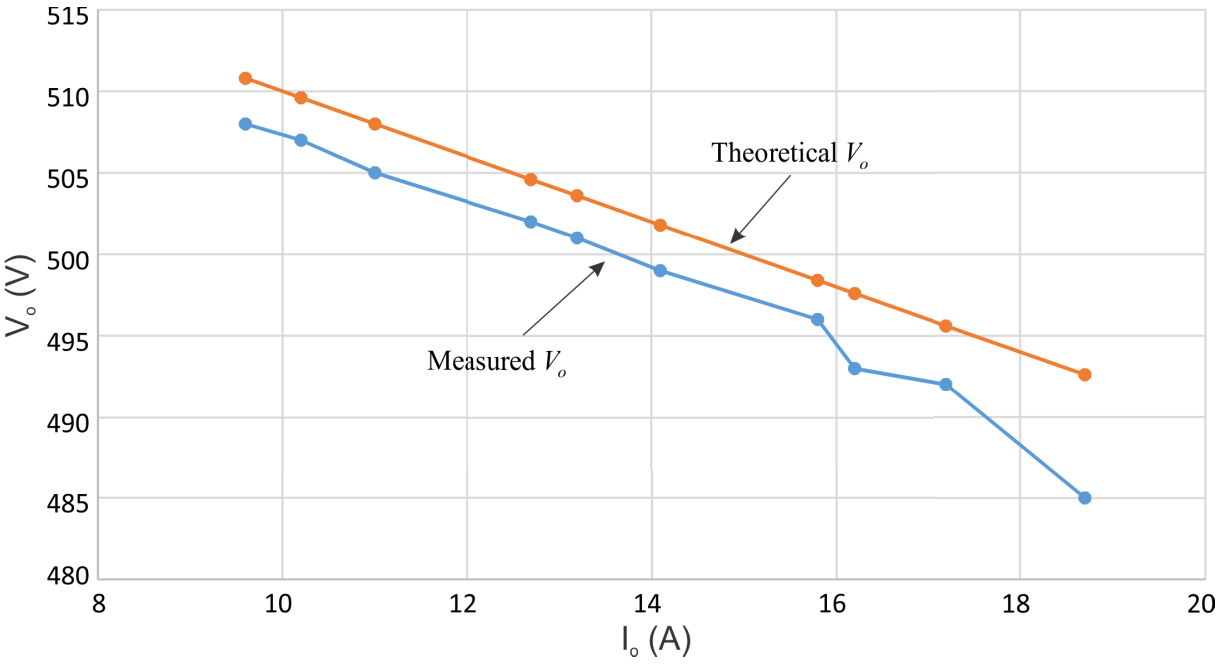
Source: Own Elaborated

In the first experiment, the voltage reference was configured to 530 V, and the virtual output resistance to 2 Ω. The input voltage was set at 600 V, to the converter operate in Buck Mode. The results are presented in Table 9.2 and Figure 9.15.

Table 9.2 – Experimental Results Data - Virtual Resistance in Buck Mode

I_o **(A)**	**Measured** V_o **(V)**	**Theoretical** V_o **(V)**	**Error**
9.6	508	510.8	0.548%
10.2	507	509.6	0.510%
11.0	505	508.0	0.591%
12.7	502	504.6	0.515%
13.2	501	503.6	0.516%
14.1	499	501.8	0.558%
15.8	496	498.4	0.482%
16.2	493	497.6	0.924%
17.2	492	495.6	0.726%
18.7	485	492.6	1.543%

Figure 9.15 – Experimental Results - Virtual Resistance in Buck Mode



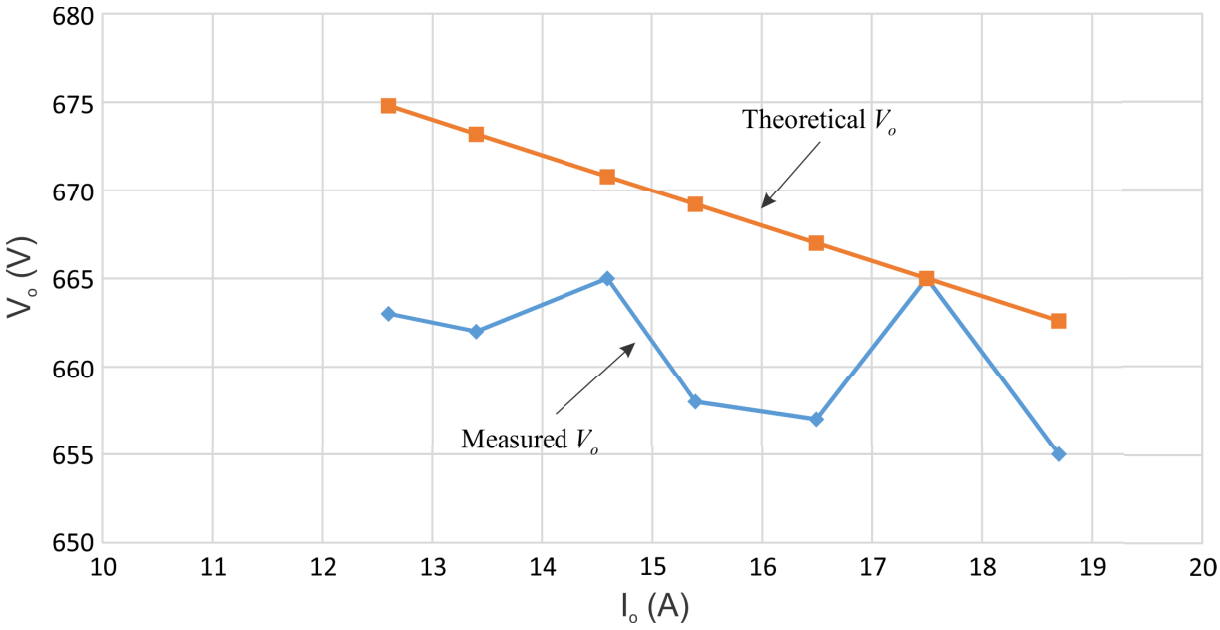
It can be observed that the output voltage is reducing according to the current increase, showing the effect of the virtual resistance. The maximum error found in this experiment is less than two percent.

The second experiment was configured for the converter to operate in Boost mode. Then, the reference voltage was configured at 700 V, the virtual resistance at 2 Ω, and the input voltage at 500 V. The results are shown in Table 9.3 and Figure 9.16.

Table 9.3 – Experimental Results Data - Virtual Resistance in Boost Mode

Measured I_o (A)	**Measured V_o (V)**	**Theoretical V_o (V)**	**Error**
12.6	663	674.8	1.749%
13.4	662	673.2	1.664%
14.6	665	670.8	0.865%
15.4	658	669.2	1.674%
16.5	657	667.0	1.499%
17.5	665	665.0	0.000%
18.7	655	662.6	1.147%

Figure 9.16 – Experimental Results - Virtual Resistance in Boost Mode



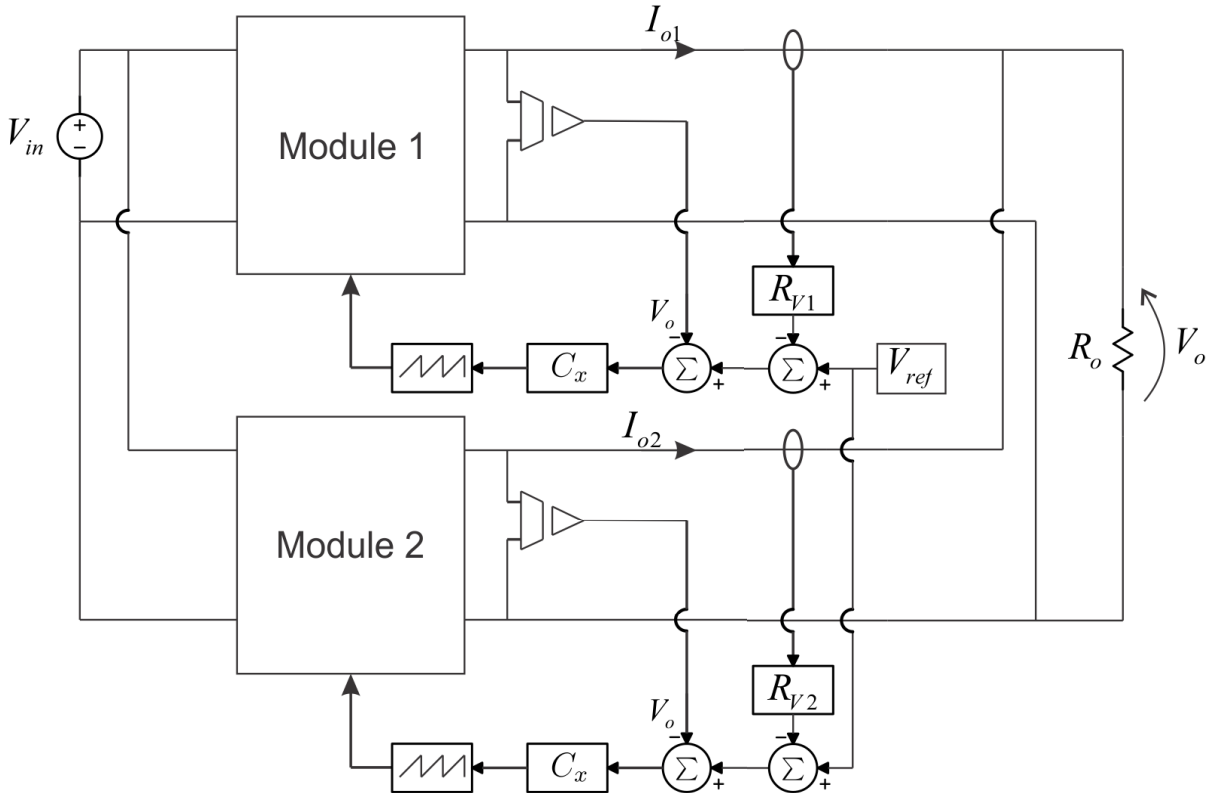
Similarly to Buck mode, the error found for Boost operation is less than two percent.

In both cases, it can be noticed the addition of a virtual resistance in the control loop. Once implemented, it is possible to set both converters in parallel, using the droop method.

9.3 PARALLELING CONVERTERS - DROOP CONTROL

To set both converters in parallel, the virtual resistances were implemented in both, as the structure is shown in Figure 9.17. In the experiments, the power supply was shared, and the output voltage reference was the same for the two modules. Then, different scenarios were created for the given parameters.

Figure 9.17 – Test Setup - Virtual Resistances



Source: Own Elaborated

Table 9.4 and Figure 9.18 show the results for $V_{in} = 700V$; $V_{ref} = 500V$; $R_{V1} = R_{V2} = 4\Omega$.

Table 9.4 – Experimental Results Data - Droop Control 01

V_o	**Module 1 Current (A)**	**Module 2 Current (A)**	**Theoretical Current (A)**	**Error Module 1**	**Error Module 2**
464	8.8	8.9	9.00	2.22%	1.67%
467	8.2	8.2	8.25	0.61%	1.09%
468	7.9	7.8	8.00	1.25%	3.13%
470	7.5	7.5	7.50	0.00%	0.40%
473	6.9	6.8	6.75	-2.22%	-0.15%
474	6.4	6.4	6.50	1.54%	2.31%
476	6.2	6.1	6.00	-3.33%	-1.17%
479	5.6	5.4	5.25	-6.67%	-2.10%
481	5.1	4.9	4.75	-7.37%	-3.79%
482	4.9	4.6	4.50	-8.89%	-2.89%

Figure 9.18 – Experimental Results - Droop Control 01

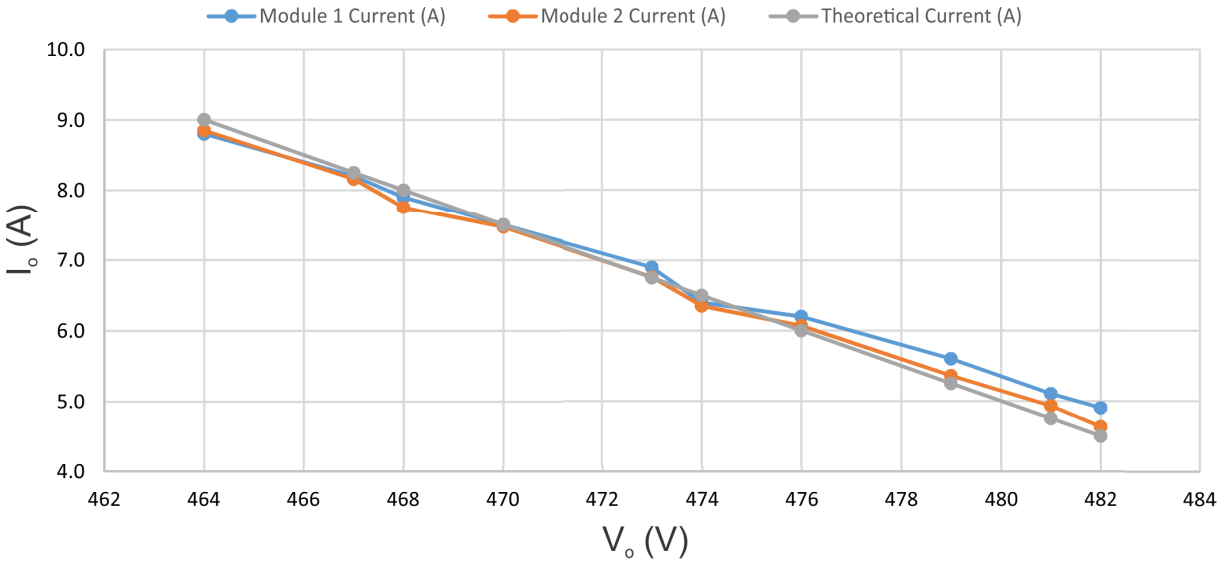


Table 9.5 and Figure 9.19 show the results for $V_{in} = 600V$; $V_{ref} = 550V$; $R_{V1} = R_{V2} = 4\Omega$.

Table 9.5 – Experimental Results Data - Droop Control 02

V_o	**Module 1 Current (A)**	**Module 2 Current (A)**	**Theoretical Current (A)**	**Error Module 1**	**Error Module 2**
529	5.1	5.0	5.25	2.86%	4.00%
528	5.3	5.4	5.50	3.64%	2.73%
526	5.9	5.8	6.00	1.67%	2.83%
525	6.1	6.1	6.25	2.40%	1.76%
523	6.5	6.6	6.75	3.70%	2.37%
522	6.8	6.9	7.00	2.86%	1.43%
520	7.3	7.4	7.50	2.67%	2.00%

Figure 9.19 – Experimental Results - Droop Control 02

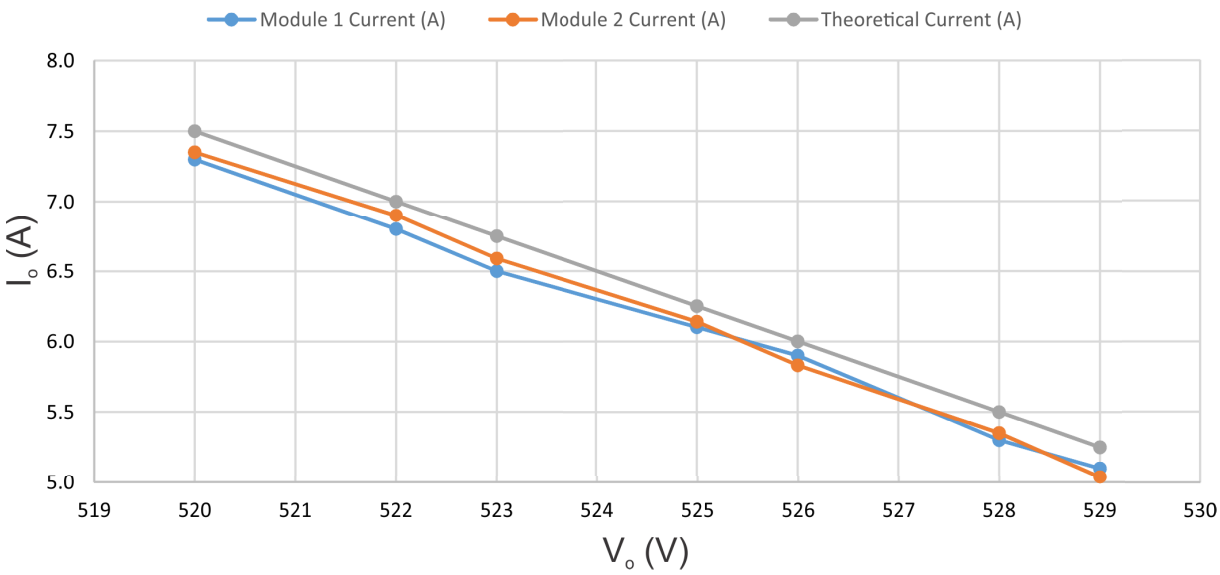


Table 9.6 and Figure 9.20 show the results for $V_{in} = 500V$; $V_{ref} = 600V$; $R_{V1} = R_{V2} = 4\Omega$.

Table 9.6 – Experimental Results Data - Droop Control 03

V_o	**Module 1 Current (A)**	**Module 2 Current (A)**	**Theoretical Current (A)**	**Error Module 1**	**Error Module 2**
574	5.8	5.9	6.50	10.77%	9.85%
573	6.1	6.2	6.75	9.63%	8.15%
571	6.5	6.7	7.25	10.34%	7.31%
570	7.0	7.1	7.50	6.67%	5.73%
568	7.4	7.6	8.00	7.50%	5.50%
568	7.5	7.6	8.00	6.25%	5.63%
566	7.8	8.0	8.50	8.24%	5.41%

Figure 9.20 – Experimental Results - Droop Control 03

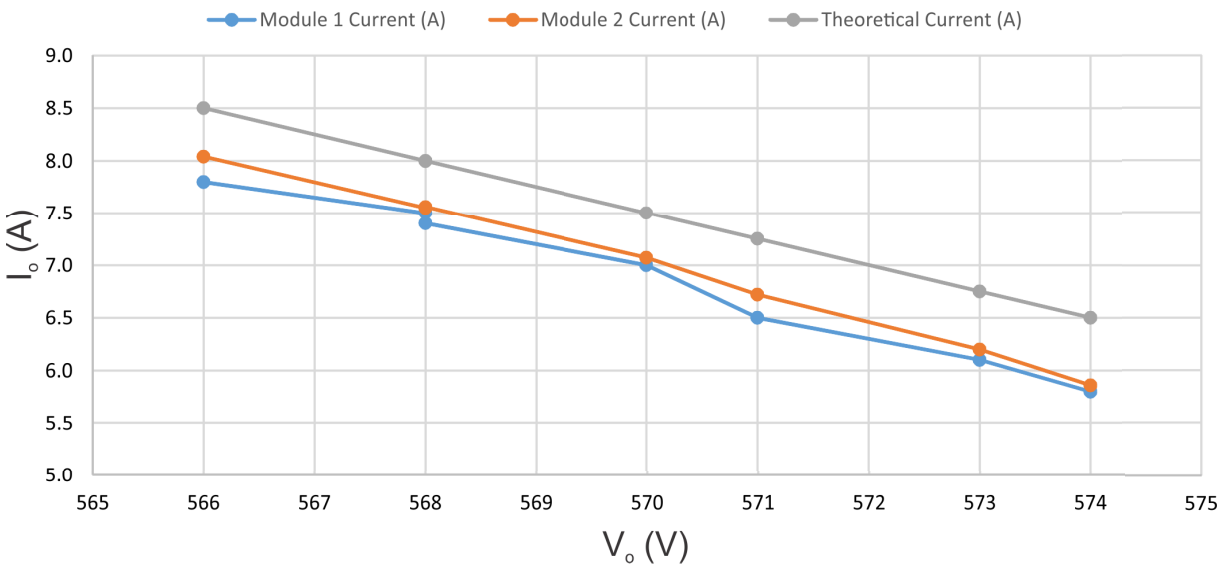


Table 9.7 and Figure 9.21 show the results for $V_{in} = 500V$; $V_{ref} = 650V$; $R_{V1} = R_{V2} = 4\Omega$.

Table 9.7 – Experimental Results Data - Droop Control 04

V_o	**Module 1 Current (A)**	**Module 2 Current (A)**	**Theoretical Current (A)**	**Error Module 1**	**Error Module 2**
614	8.6	8.7	9.00	4.44%	3.67%
616	8.2	8.1	8.50	3.53%	4.24%
617	8.0	7.8	8.25	3.03%	5.70%
618	7.7	7.7	8.00	3.75%	3.25%
620	7.5	7.2	7.50	0.00%	3.47%
621	6.8	6.7	7.25	6.21%	7.72%
623	6.3	6.3	6.75	6.67%	6.22%

Figure 9.21 – Experimental Results - Droop Control 04

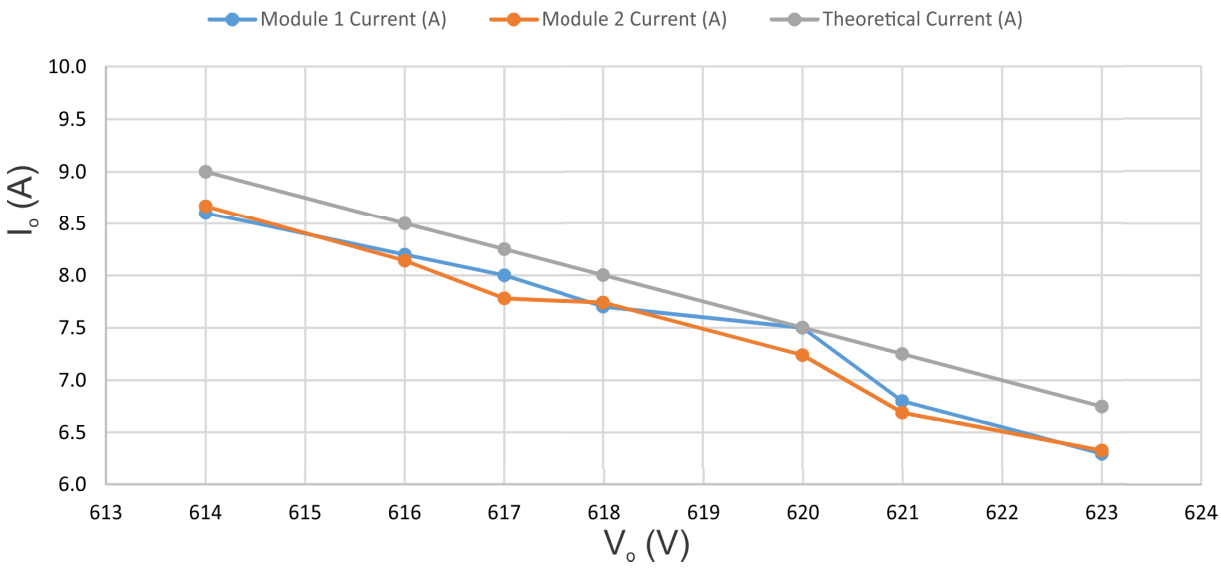


Table 9.8 and Figure 9.22 show the results for $V_{in} = 700V$; $V_{ref} = 600V$; $R_{V1} = 4\Omega$; $R_{V2} = 6\Omega$.

Table 9.8 – Experimental Results Data - Droop Control 05

V_o	**Module 1 Current (A)**	**Module 2 Current (A)**	**Theoretical Current 1 (A)**	**Theoretical Current 2 (A)**	**Error Module 1**	**Error Module 2**
561	9.0	7.9	9.75	6.50	7.69%	-21.69%
563	8.7	7.4	9.25	6.17	5.95%	-20.65%
565	8.2	7.1	8.75	5.83	6.29%	-21.54%
567	7.6	6.6	8.25	5.50	7.88%	-20.36%
569	7.2	6.3	7.75	5.17	7.10%	-21.74%
571	6.8	5.8	7.25	4.83	6.21%	-20.00%
573	6.4	5.5	6.75	4.50	5.19%	-21.78%

Figure 9.22 – Experimental Results - Droop Control 05

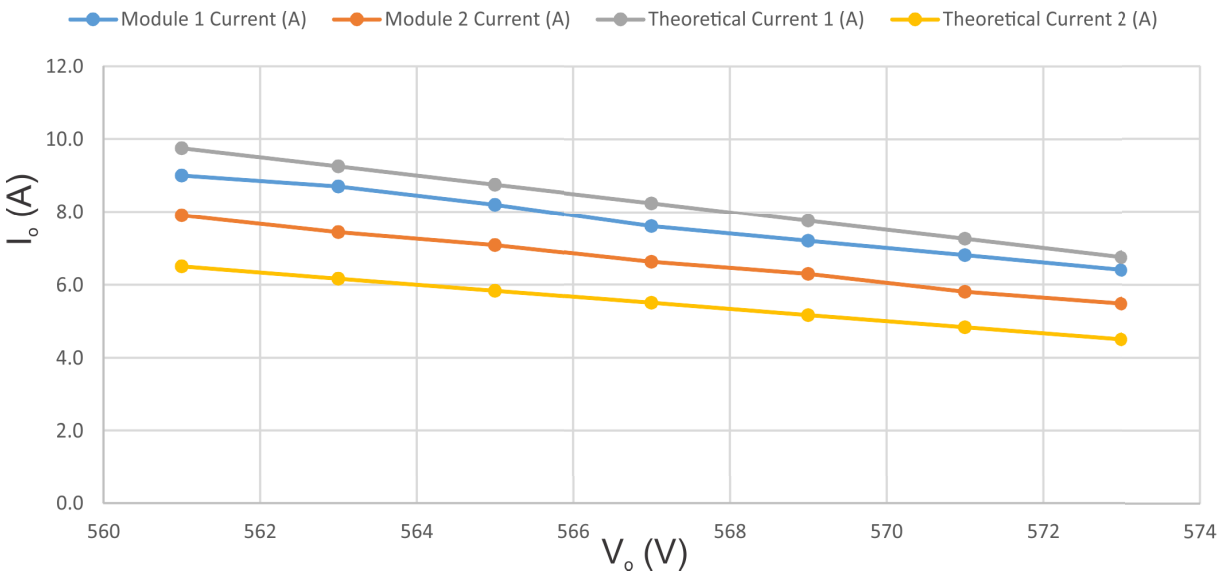
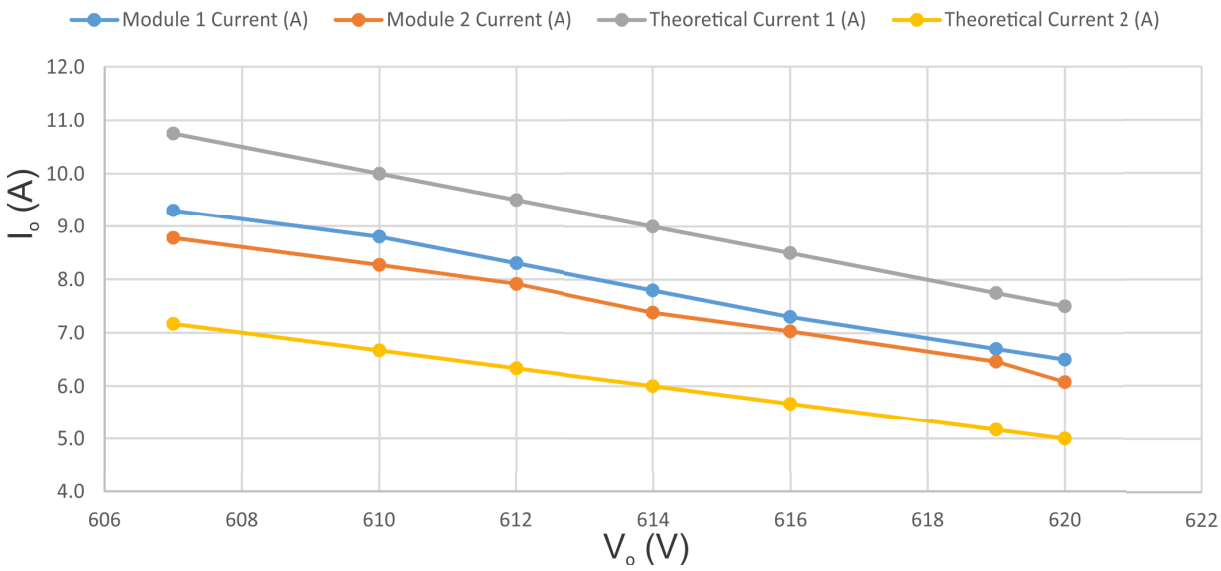


Table 9.9 and Figure 9.23 show the results for $V_{in} = 550V$; $V_{ref} = 650V$; $R_{V1} = 4\Omega$; $R_{V2} = 6\Omega$.

Table 9.9 – Experimental Results Data - Droop Control 06

V_o	**Module 1 Current (A)**	**Module 2 Current (A)**	**Theoretical Current 1 (A)**	**Theoretical Current 2 (A)**	**Error Module 1**	**Error Module 2**
620	6.5	6.1	7.50	5.00	13.33%	-21.60%
619	6.7	6.5	7.75	5.17	13.55%	-25.02%
616	7.3	7.0	8.50	5.67	14.12%	-24.05%
614	7.8	7.4	9.00	6.00	13.33%	-23.00%
612	8.3	7.9	9.50	6.33	12.63%	-24.90%
610	8.8	8.3	10.00	6.67	12.00%	-24.04%
607	9.3	8.8	10.75	7.17	13.49%	-22.51%

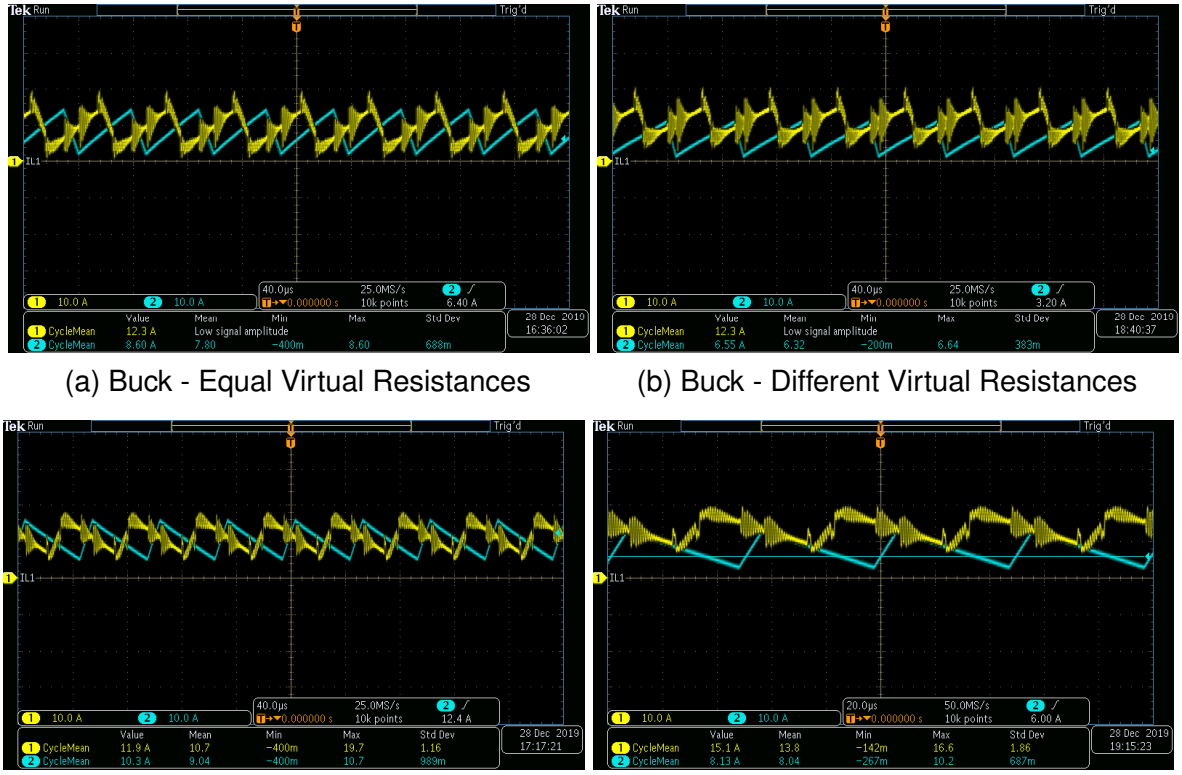
Figure 9.23 – Experimental Results - Droop Control 06



In the experiments presented from Figure 9.18 to 9.23, the effect of the virtual resistances and the droop control could be noted. The elevated percentage of error noted mostly in Figure 9.23 is the result of uncertain reading measurements of the sensors of the circuit. Also, the precision of the equipment used to take the measurements accounted for these results. On the other hand, those errors did not compromise the experimental verification of the theory presented.

The oscilloscope images shown in Figure 9.24 presents the effect of the virtual resistances on the main inductor of each module. It can be verified a high frequency noise at the channel 1 at Figure 9.24. It is the result of the lower quality of the current probe than used in channel 2.

Figure 9.24 – Inductor Currents



(a) Buck - Equal Virtual Resistances

(b) Buck - Different Virtual Resistances

(c) Boost - Equal Virtual Resistances

(d) Boost - Different Virtual Resistances

9.4 PARTIAL CONCLUSIONS

This chapter highlighted the experimental results of the designed converter and its control. First, it was verified its waveforms on semiconductors and inductor. There was an individual analysis of Buck and Boost operation, checking its performance.

Then, the virtual resistances were implemented to validate the concept and compare it with theory. Once virtual resistances were implemented in each converter, the droop control technique could be verified.

Despite presenting large percentage errors in some scenarios, droop control proved to be efficient to place converters in parallel, without the need for communication between modules, also with the simplicity of implementation.

10 CONTRIBUTIONS AND FINAL CONSIDERATIONS

A study of the parallelism of two similar Non-Inverting Buck-Boost of 30 kW each operating in CCM, to be applied in the energy transfer among battery banks were presented. Also, the theory and deduced equations were validated through the experimental results.

Combining the step-down and step-up characteristics of the Buck and Boost respectively, it was possible to design a converter to transfer energy between battery banks, without inverting the output voltage of the converters.

Different modulation techniques were presented, as well it was deduced the equations to compare and check the most advantageous operation. It can be inferred that efficiency could be improved by using level-shifted carriers, which reduces the power loss in the semiconductors.

The interleaving strategy adds up as a differential for paralleling modules, which helps to reduce the size of the converter output filters. This is achieved by increasing the apparent frequency and reducing the electrical current efforts on passive elements.

Finally, virtual resistances and droop control were introduced as an easy method to connect converters in parallel, avoiding the need of communication amid them. After, the theory presented was validated through experimental results with the equalization of the currents.

During the execution of the work, several difficulties for the implementation of the project arose. Meeting the technical specifications, the available budget, the local availability, and the time for research brought challenges.

One of the obstacles faced during the research was the purchase of semiconductors. There are currently power modules on the market that facilitate the design of the converter, together with an arrangement that helps to cool the assembly. The availability of these modules, however, is linked to terms of approximately 20 weeks, which is equivalent to 5 months. This, in a way, goes against the master's development deadlines. Therefore, the option was to purchase discrete components, which increased the volume of the converter.

The use of discrete components made semiconductor parallelism necessary, so that the junction temperatures do not exceed the values ??informed in the manufacturer's datasheet. The model chosen, in turn, was not something that brought difficulties, since the chosen components had a positive temperature coefficient, allowing a natural equalization of the components.

Another difficulty encountered was the fabrication of the converter structure. Thermal calculations showed the need for heatsinks with low thermal resistance. The option found was the use of aluminum sinks with forced ventilation, which significantly increased the size of the modules. The use of refrigeration through liquid cooling was

considered, but there is no supply of the product in the country.

All of this made the construction of the converter a handmade process. Various construction techniques have been verified in order to improve the requirements of the project. The conductors used to interconnect the power part were copper bars. Such an option ended up causing parasitic inductances in the converter structure, which generated overvoltages in the semiconductors. These had to be adjusted through the gate resistors, decreasing the efficiency of the converter. Another problem when using copper bars is the electromagnetic interference generated, which affected analog measurements and was perceived, even, in the vicinity of the converter. This had a major impact on the command of the gates drivers, which were being influenced by the switching, even causing the semiconductor to switch twice within a switching period. To solve the problem, it was necessary to improve the connection between the gate driver and the semiconductors. Even so, due to the structure of the converter being metallic, the effects were still perceived in the gate signals.

However, once the converter was installed, which was operating without obstacles under the specified conditions, other difficulties appeared. To implement the control, analog readings must be guaranteed. Even when sizing analog filters through resistors, capacitors, and operational amplifiers, the response obtained in measurements was different. For example, a filter with the same cutoff frequency, but with the combination of different capacitor and resistor values, had a different signal filter quality. Therefore, adjusting the measurements was something that took a long time to enable the implementation of the control.

Thus, it is clear that, while the project is in a simulation environment, everything becomes simple and possible. In the implementation process, the non-idealities of the components and the way they affect the project are perceived.

- to build the final product with the ten-level converter, totalizing 300 kW;
- to verify the efficiency of interleaved converters;
- to perform a transient analysis (step response) of the control;
- to implement and to test the converters with batteries, respecting their voltage and current limits;
- to reduce the size of the converter, by choosing different semiconductors and improving the cooling system;
- To improve digital measurements on the microprocessor in order to obtain more accurate results through the control loop.

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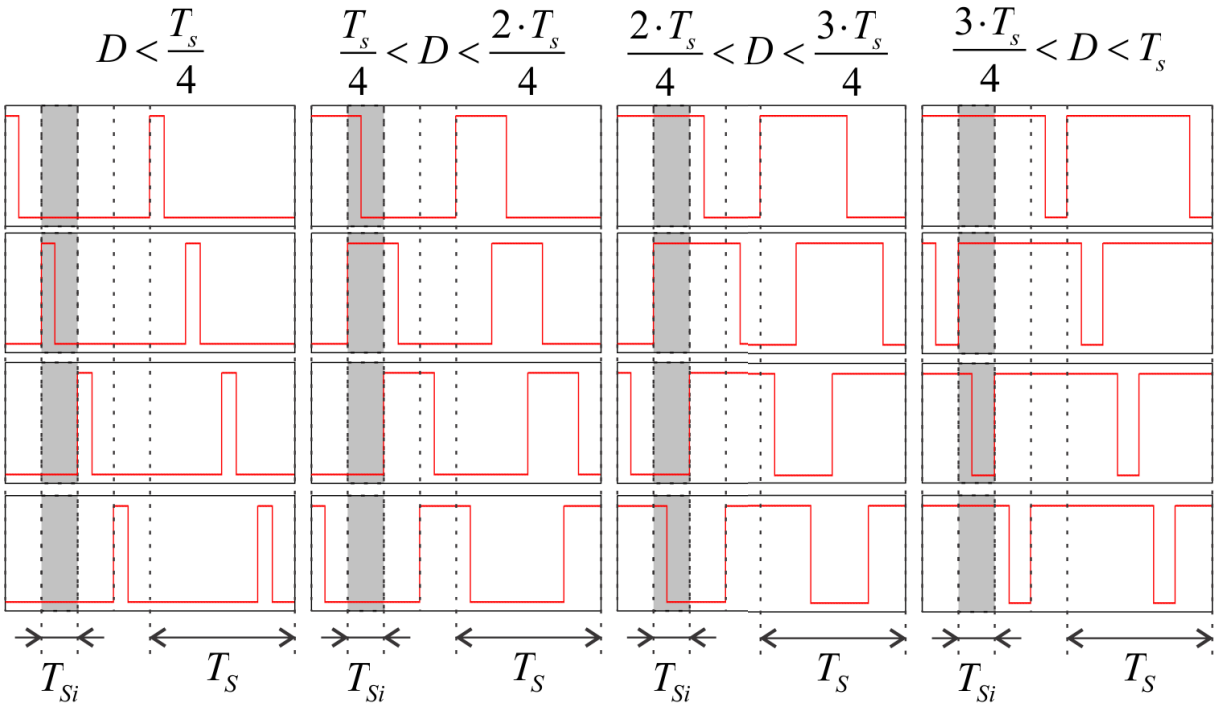
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APPENDIX A – INTERLEAVING OPERATION

Converters operating in interleaving allows the size reduction of input and output filters, because they depending of its operating frequency and ripple. To find new equations to describe the values over the filters, it is necessary to evaluate each scenario that the converter will operate. In this Appendix will be presented relations and equations that will help to determine equations for interleaved converters.

For a given number "*n*" of levels, it may present "*n*" scenarios. Figure A.1 presents the possible duty cycle operations for a four level interleaved converter: (*i*) duty cycle lower than $\frac{1}{4}$; (*ii*) duty cycle between $\frac{1}{4}$ and $\frac{2}{4}$; (*iii*) duty cycle between $\frac{2}{4}$ and $\frac{3}{4}$; (*iv*) duty cycle greater than $\frac{3}{4}$. From this data, it is possible to obtain Table A.1, which relates the number of switches ON n_{on}, switches OFF n_{off}, given the duty cycle applied. It is also defined the new virtual period T_{Si}, and the virtual duty cycle D_i.

Figure A.1 – Four level switching command



Source: Own elaborated

From Figure A.1, the virtual duty cycle D_i, which is helpful to determine the equations that describes ripples in interleaved converters. Table A.1 presents the number of switches open and closed in the interval T_{Si}.

$$T_{Si} = \frac{T_S}{n} \tag{A.1}$$

Table A.1 – Four level Analysis

Scenario	**Duty Cycle**	n_{on}	n_{off}	D_i
(i)	$D < \frac{1}{4}$	0	3	$4(D)$
(ii)	$\frac{1}{4} < D < \frac{2}{4}$	1	2	$4(D - \frac{1}{4})$
(iii)	$\frac{2}{4} < D < \frac{3}{4}$	2	1	$4(D - \frac{2}{4})$
(iv)	$D > \frac{3}{4}$	3	0	$4(D - \frac{3}{4})$

Source: Own elaborated

In scenario (*i*) one switch is changing state while three are open during all interval. Scenario (*ii*) one switch are closed, while two are open. Scenario (*iii*) two switches are closed while one is open. Scenario (*iv*) three switches are closed while none is open.

Similarly, it is possible to create a generic table for a n-level converter.

Table A.2 – N-level Analysis

Duty Cycle	n_{on}	n_{off}	D_i
$D < \frac{1}{n}$	0	$n-1$	$n(D)$
$\frac{1}{n} < D < \frac{2}{n}$	1	$n-2$	$n(D - \frac{1}{n})$
...	...	...	...
$\frac{n-2}{n} < D < \frac{n-1}{n}$	$n-2$	1	$n(D - \frac{n-2}{n})$
$\frac{n-1}{n} < D < 1$	$n-1$	0	$n(D - \frac{n-1}{n})$

Source: Own elaborated

From Table A.2, it is possible to find equations which relate the ON and OFF switches according with a given duty cycle and the number of interleaved converters.

The number of closed switches in the virtual interval T_{Si} is equal to the floor number result of levels times the duty cycle, as shown in equation (A.2).

$$n_{on} = \lfloor n \cdot D \rfloor \tag{A.2}$$

The number of open switches are given by:

$$n_{off} = n - n_{on} - 1 \tag{A.3}$$

The virtual duty cycle D_i can be described as:

$$D_i = n \cdot D - n_{on} \tag{A.4}$$

It is important to remember that those equations are only valid when the phase shift between the carriers are the same. In other words the phase shift among all interleaved converters must be the switching period divided by the number of converters. Also, it is considered that all converters are in the same switching frequency.

ANNEX A – INDUCTOR PROJECT CALCULATIONS

Projeto de Indutor

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Rev: 10/08/19

Dados do Indutor

Potência de um módulo $P_o := 30kW$

Tensão mínima $V_{min} := 520V$

Frequência de operação $f_s := 20kHz$

Corrente média no Indutor $I := \frac{P_o}{V_{min}} = 57.692\,A$

Ondulação de Corrente $\Delta I := 20A$

Corrente de Pico $I_p := I + \frac{\Delta I}{2} = 67.692\,A$

Corrente Eficaz $I_{ef} := 41.36A$

Indutância desejada $L_{bb} := \frac{0.456}{4}mH = 114 \cdot \mu H$

Núcleo TIPO EE - 76/50/76

Permissividade inicial

$$\mu_i := 2100$$

Densidade máxima de Fluxo magnético

$$B_{max} := 0.3T$$

Máxima densidade de corrente elétrica

$$J_{max} := 450\,\frac{A}{(cm)^2}$$

Fator de Enrolamento

$$k_w := 0.6$$

AeAw Mínimo

$$AeAw := \frac{L_{bb}\cdot I_p\cdot I_{ef}}{k_w\cdot B_{max}\cdot J_{max}} = 39.404\cdot(cm)^4$$

Variação de Densidade de Fluxo

$$\Delta B := B_{max}\cdot\frac{\Delta I}{I_p} = 0.089\,T$$

Nucleo Thonrton 76/50/76

Quantidade de núcleos em paralelo

$$N_n := 1$$

$$A_e := N_n\cdot 1935.48\,(mm)^2 = 1.935\times 10^3\cdot(mm)^2$$

$$A_w := \frac{(50.8 - 25.4)}{2}\cdot 38.1\cdot 2\cdot(mm)^2$$

AeAw do Núcleo

$$AeAw2 := A_e\cdot A_w = 187.304\cdot(cm)^4$$

Número de espiras necessárias

$$N_e := ceil\left(\frac{L_{bb}\cdot I_p}{B_{max}\cdot A_e}\right) = 14$$

Cálculo do Entreferro

Entreferro Total

$$l_{g_t} := \frac{N_e^{\,2}\cdot \mu_0 \cdot A_e}{L_{bb}} = 0.418\cdot cm$$

Entreferro

$$l_{g2} := \frac{l_{g_t}}{4} = 1.045\cdot mm$$

Cálculo do Cobre

Diâmetro do Efeito pelicular

$$\Delta := \frac{2\cdot 7.5}{\sqrt{f_s}}\cdot s^{\frac{-1}{2}}\cdot cm = 0.106\cdot cm$$

Escolhendo o fio AWG18 d=0.102cm

Área do Cobre

$$S\Delta := 0.008231 cm^2$$

Seção necessária para capacidade de corrente

$$S_L := \frac{I_{ef}}{J_{max}} = 0.092\cdot cm^2$$

Número de Condutores em paralelo

$$N_{cond_p} := ceil\left(\frac{S_L}{S\Delta}\right) = 12$$

Área do cobre + esmalte do AWG28

$$S\Delta_e := 0.009735 cm^2$$

Núcleo EE76/50/76

Para ser executável o projeto, a ocupação deve ser superior a 0.3 e inferior a 1.

$$k_{u2} := \frac{\left[\left(S\Delta_e\cdot N_{cond_p}\right)\cdot N_e\right]}{A_w\cdot k_w} = 0.282$$

Perdas no Cobre

Comprimento médio de 1 espira no condutor

$$l_{espira} := N_n \cdot (40 + 100) \cdot 2mm = 0.28\,m$$

Comprimento total de cobre

$$l_t := N_e \cdot l_{espira} = 3.92\,m$$

Resistividade do Cobre

$$\rho_{cu} := 0.0171\Omega \cdot \frac{mm^2}{m}$$

Resistividade do Fio

$$R_f := \frac{\left(\rho_{cu} \cdot l_{espira} \cdot N_e\right)}{S\Delta \cdot N_{cond_p}} = 6.787 \times 10^{-3} \cdot \Omega$$

Perdas no cobre

$$P_{cu} := R_f \cdot {I_{ef}}^2 = 11.609\,W$$

Perdas Magnéticas

Coeficiente de Perdas por Histerese

$$K_h := 4 \cdot 10^{-5} \frac{(W \cdot s)}{cm^3}$$

Coeficiente de Perdas por correntes parasitas

$$K_f := 4 \cdot 10^{-10} \frac{\left(W \cdot s^2\right)}{cm^3}$$

Volume total do núcleo

$$V_{nucleo2} := N_n \cdot 421350.1mm^3 = 421.35 \cdot cm$$

Perda total no Núcleo

$$P_{nuc} := \left(\frac{\Delta B}{T}\right)^{2.4} \cdot \left(K_h \cdot f_s + K_f \cdot f_s^2\right) \cdot V_{nucleo2} = 1.206 \cdot W$$

Resistência Térmica do Núcleo

Resistência Térmica do Núcleo

$$R_{t_nucleo} := 23 \cdot \left(\frac{A_e \cdot A_W}{cm^4} \right)^{-0.37} \cdot \frac{K}{W} = 3.318 \cdot \frac{K}{W}$$

Elevação de Temperatura do Núcleo

$$\Delta T_2 := \left(P_{cu} + P_{nuc} \right) \cdot R_{t_nucleo} = 42.521 \cdot \Delta °C$$

ANNEX B – SOURCE CODE

```
/*
 *              UNIVERSIDADE FEDERAL DE SANTA CATARINA
 *              CENTRO TECNOLOGICO
 *              DEPARTAMENTO DE ENGENHARIA ELETRICA
 *              LABORATORIO FOTOVOLTAICA
 *
 *              AUTOR: JOAO MARTINS JUNIOR
 *              DATA: 15/12/2019
 *
 *              ALGORITMO PARA CONTROLE DE CARREGADOR RAPIDO DE BATERIAS LITIO
 *              DISSERTACAO DE MESTRADO
 *
 */

//      BIBLIOTECAS

#include "DSP28x_Project.h"

__interrupt void adc_isr(void);
void Adc_Config(void);
void configADC(void);


//      DEFINICOES

#define fs 20000
#define ts 4499
#define ph 2249
#define dutyBuckSupD 0
#define dutyBoostSupD 0
#define dutyBuckInfD 0
#define dutyBoostInfD 0

//      VARIAVEIS GLOBAIS

float dutySup = 0;
float dutyInf = 0;
float dutyBuckSupS = 0;
float dutyBoostSupS = 0;
float dutyBuckInfS = 0;
float dutyBoostInfS = 0;


float Vin = 0;
float Vo =  0;
float Io_sup = 0;
float Iin_sup = 0;
float Io_inf = 0;
float Iin_inf = 0;

float dutyInf_ant = 0;
float erroInf = 0;
float erroInf_ant = 0;
float RvInf = 4;

float dutySup_ant = 0;
float erroSup = 0;
float erroSup_ant = 0;
float RvSup = 4;


float Vref = 0;

float a0 = -0.2126362386;
float a1 = 0.2133637614;
```

```
67.
68. //      FUNCOES
69.
70. //void configGPIO(void);
71. void configPWM(void);
72.
73.
74. /**
75.  * main.c
76.  */
77. int main(void)
78. {
79.     InitGpio();             // Configura as GPIO's
80.     InitSysCtrl();          //configura os registradores de controle do sistema
81.
82.     // Step 1. Initialize System Control:
83.     // PLL, WatchDog, enable Peripheral Clocks
84.     // This example function is found in the F2806x_SysCtrl.c file.
85.         InitSysCtrl();
86.
87.     // Step 2. Initialize GPIO
88.     //configGPIO();
89.
90.     //Step 3. Clear all interrupts and initialize PIE vector table:
91.     // Disable CPU interrupts
92.        DINT;
93.
94.     // Initialize the PIE control registers to their default state.
95.     // The default state is all PIE interrupts disabled and flags are cleared.
96.     // This function is found in the F2806x_PieCtrl.c file.
97.        InitPieCtrl();
98.
99.      // Disable CPU interrupts and clear all CPU interrupt flags;
100.       IER = 0x0000;
101.       IFR = 0x0000;
102.
103.    // Initialize the PIE vector table with pointers to the shell Interrupt
104.    // Service Routines (ISR).
105.    // This will populate the entire table, even if the interrupt
106.    // is not used in this example.  This is useful for debug purposes.
107.    // The shell ISR routines are found in F2806x_DefaultIsr.c.
108.    // This function is found in F2806x_PieVect.c.
109.       InitPieVectTable();
110.
111.    // Interrupts that are used in this example are re-mapped to
112.    // ISR functions found within this file.
113.       EALLOW; // This is neede to write to EALLOW protected register
114.       PieVectTable.ADCINT1 = &adc_isr;
115.       EDIS; // This is needed to disable write to EALLOW protected registers
116.
117.    // Step 4. Initialize all the Device Peripherals;
118.
119.       InitAdc(); //For this example, init the ADC
120.       AdcOffsetSelfCal();
121.
122.    // Step 5. User specific code, enable interrupts;
123.
124.    // Enable ADCINT1 in PIE
125.       PieCtrlRegs.PIEIER1.bit.INTx1 = 1; //Enable INT 1.1 in the PIE
126.       IER |= M_INT1;   // Enable CPU Interrupt 1
127.       EINT;    // Enable Global interrupt INTM
128.       ERTM;    // Enable Global realtime interrupt DBGM
129.
130.
131.   // Wait for ADC interrupt
132.       configPWM();
```

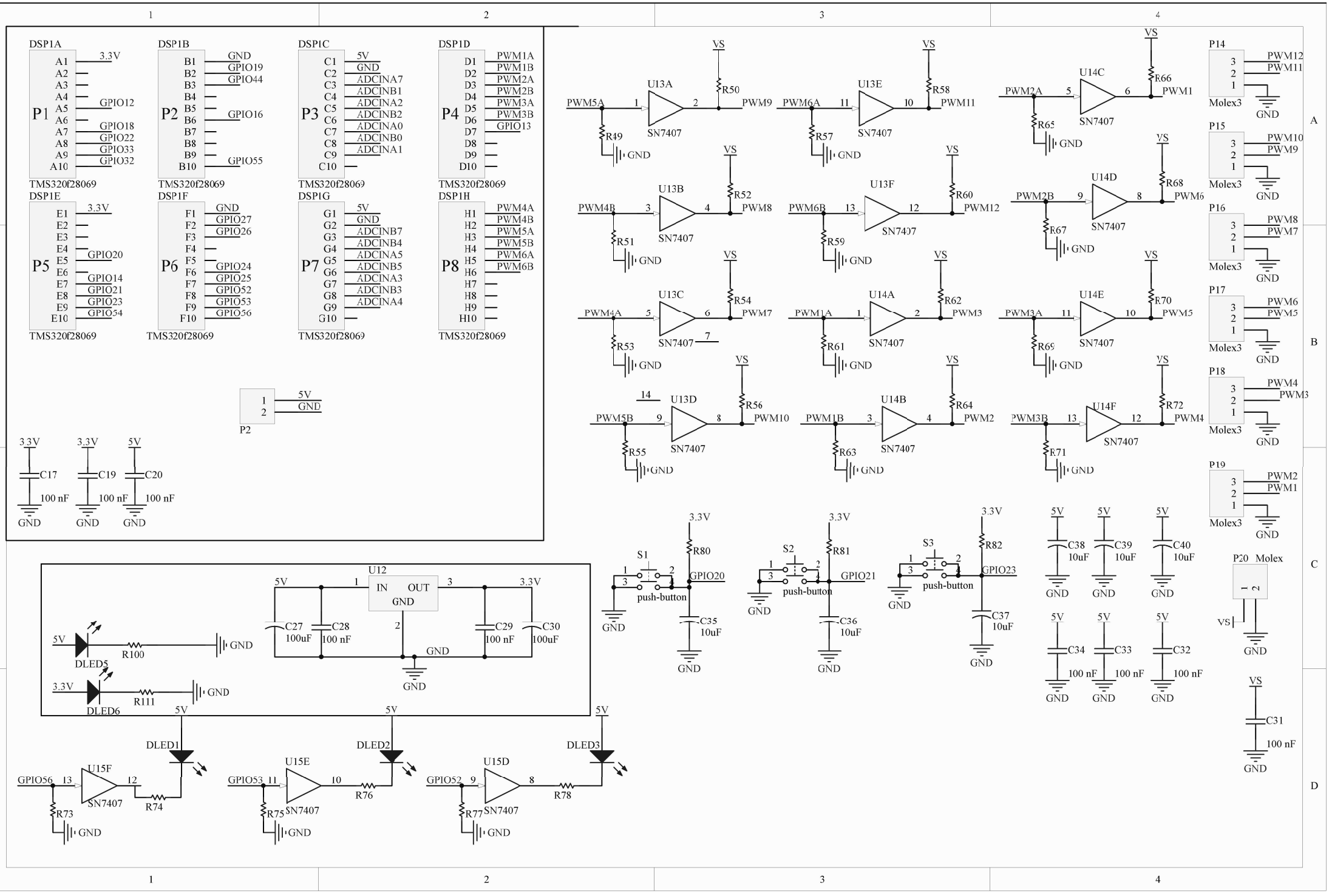
```
133.
134.
135.    // ADC and ePWM configuration
136.       configADC();
137.
138.
139.    while(1){}
140.
141. }
142.
143.
144.
145.__interrupt void adc_isr(void)
146.{
147.
148.//  Leituras
149.
150.    Vo =      (((float)AdcResult.ADCRESULT1*0.22) - 0.747);
151.
152.    Io_inf =  (((float)AdcResult.ADCRESULT2*0.0344) - 36.4);
153.
154.    Io_sup=   (((float)AdcResult.ADCRESULT3*0.0187) - 26.4);
155.
156.
157.//  Controlador Digital Inferior
158.
159.    erroInf = Vref - Vo - RvInf*Io_inf;
160.    dutyInf = erroInf*a1 + erroInf_ant*a0 + dutyInf_ant;
161.
162.//  Controlador Digital Superior
163.
164.    erroSup = Vref - Vo - RvSup*Io_sup;
165.    dutySup = erroSup*a1 + erroSup_ant*a0 + dutySup_ant;
166.
167.// Anti-Windup
168.
169.    if(dutyInf>6000){dutyInf = 6000;}
170.    if(dutyInf<1){dutyInf = 0;}
171.
172.    if(dutySup>6000){dutySup = 6000;}
173.    if(dutySup<1){dutySup = 0;}
174.
175.// Portadoras sobrepostas
176.
177.    if(dutySup<4499){
178.        dutyBuckSupS = dutySup;
179.        dutyBoostSupS = 0;
180.        }
181.    else{
182.        dutyBuckSupS = 4500;
183.        dutyBoostSupS = dutySup - 4499;
184.        }
185.
186.
187.    if(dutyInf<4499){
188.        dutyBuckInfS = dutyInf;
189.        dutyBoostInfS = 0;
190.        }
191.    else{
192.        dutyBuckInfS = 4500;
193.        dutyBoostInfS = dutyInf - 4499;
194.        }
195.
196.
197.// Memória
198.
```

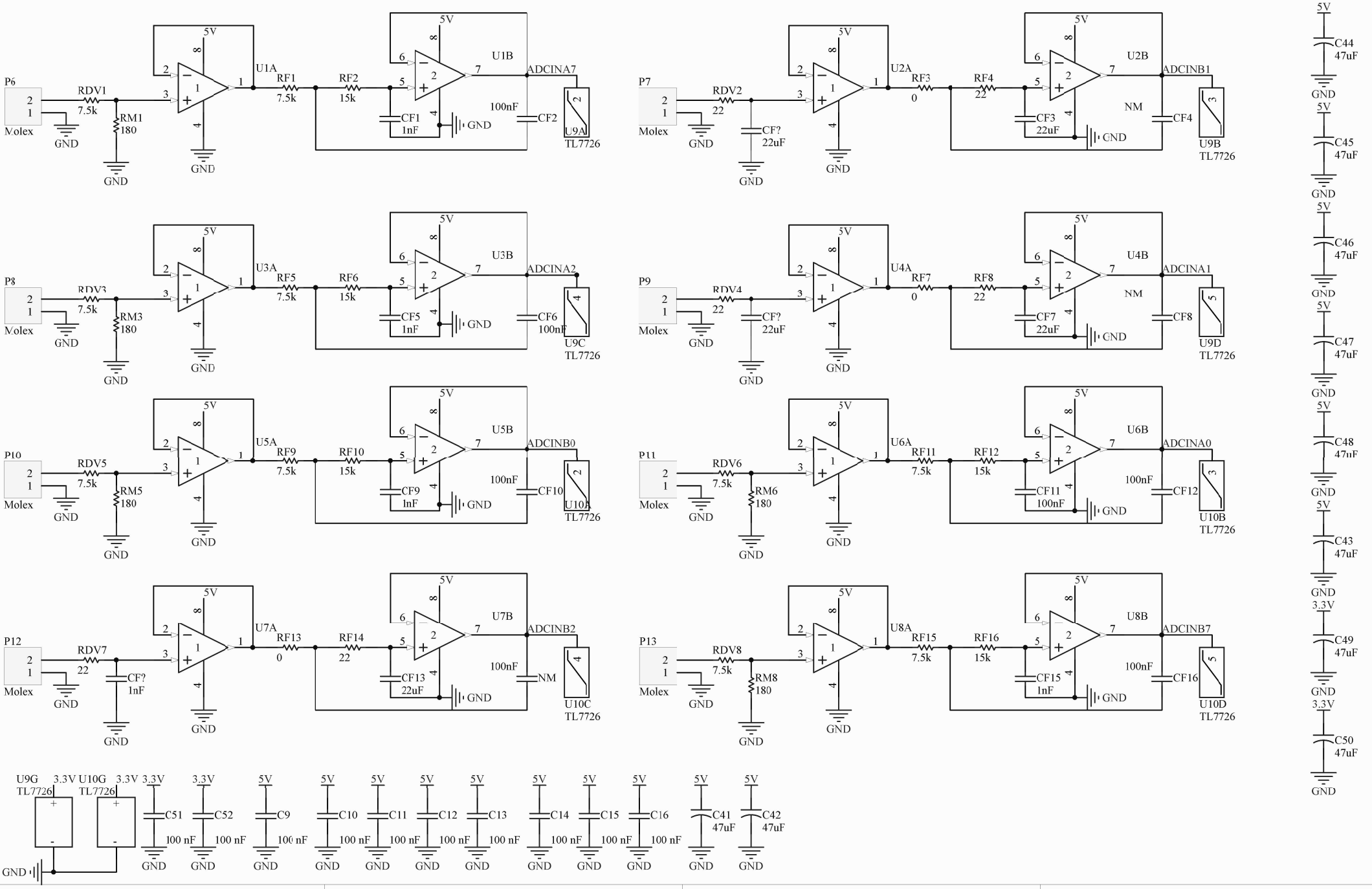
```
199.    dutyInf_ant = dutyInf;
200.    erroInf_ant = erroInf;
201.    dutySup_ant = dutySup;
202.    erroSup_ant = erroSup;
203.
204.// Atualização do duty cycle superior
205.
206.    EPwm5Regs.CMPA.half.CMPA = dutyBuckSupD;
207.    EPwm5Regs.CMPB= dutyBuckSupS;
208.    EPwm6Regs.CMPA.half.CMPA = dutyBoostSupS;
209.    EPwm6Regs.CMPB= dutyBoostSupD;
210.
211.
212.// Atualização do duty cycle inferior
213.
214.    EPwm2Regs.CMPB= dutyBuckInfS;
215.    EPwm3Regs.CMPA.half.CMPA = dutyBuckInfD;
216.    EPwm4Regs.CMPA.half.CMPA = dutyBoostInfS;
217.    EPwm4Regs.CMPB= dutyBoostInfD;
218.
219.
220.
221.    AdcRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;     //Clear ADCINT1 flag reinitialize for next
    SOC
222.    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;   // Acknowledge interrupt to PIE
223.}
224.
225.void configADC(void)
226.{
227.
228.// Configure ADC
229.    EALLOW;
230.    AdcRegs.ADCCTL2.bit.ADCNONOVERLAP = 0;  // Disable non-overlap mode
231.    AdcRegs.ADCCTL1.bit.INTPULSEPOS = 1;    // ADCINT1 trips after AdcResults latch
232.    AdcRegs.INTSEL1N2.bit.INT1E     = 1;    // Enabled ADCINT1
233.    AdcRegs.INTSEL1N2.bit.INT1CONT  = 1;    // Disable ADCINT1 Continuous mode
234.    AdcRegs.INTSEL1N2.bit.INT1SEL   = 1;    // setup EOC1 to trigger ADCINT1 to fire
235.
236.    AdcRegs.ADCCTL2.bit.CLKDIV2EN = 0;      // Define o clock do ADC. 0 = SYSCLK / 1 = S
    YSCLK/2
237.    AdcRegs.ADCCTL2.bit.CLKDIV4EN = 0;      // Também defne o clock do adc.
238.
239.
240.// Definicao de ADC - SOC1 alocado para entrada ADCINB2 - Tensao Saida
241.    AdcRegs.ADCSOC1CTL.bit.CHSEL    = 10;    // set SOC0 channel select to ADCINB2   -
242.    AdcRegs.ADCSOC1CTL.bit.TRIGSEL  = 5;     // set SOC0 start trigger on EPWM1A, due to
    round-robin SOC0 converts first then SOC1
243.    AdcRegs.ADCSOC1CTL.bit.ACQPS    = 6;     // set SOC0 S/H Window to 7 ADC Clock Cycle
    s, (6 ACQPS plus 1)
244.
245.// Definicao de ADC - SOC0 alocado para entrada ADCINA0 - Corrente Saida Mod iNF
246.    AdcRegs.ADCSOC2CTL.bit.CHSEL    = 1;     // set SOC0 channel select to ADCINA1   -
247.    AdcRegs.ADCSOC2CTL.bit.TRIGSEL  = 5;     // set SOC0 start trigger on EPWM2A, due to
    round-robin SOC0 converts first then SOC1
248.    AdcRegs.ADCSOC2CTL.bit.ACQPS    = 6;     // set SOC0 S/H Window to 7 ADC Clock Cycle
    s, (6 ACQPS plus 1)
249.
250.// Definicao de ADC - SOC0 alocado para entrada ADCINB7 - Corrente Saida mod Sup
251.    AdcRegs.ADCSOC3CTL.bit.CHSEL    = 9;    // set SOC0 channel select to ADCINB1   -
252.    AdcRegs.ADCSOC3CTL.bit.TRIGSEL  = 5;     // set SOC0 start trigger on EPWM5A, due to
    round-robin SOC0 converts first then SOC1
253.    AdcRegs.ADCSOC3CTL.bit.ACQPS    = 6;     // set SOC0 S/H Window to 7 ADC Clock Cycle
    s, (6 ACQPS plus 1)
254.
255.    EDIS;
256.
```

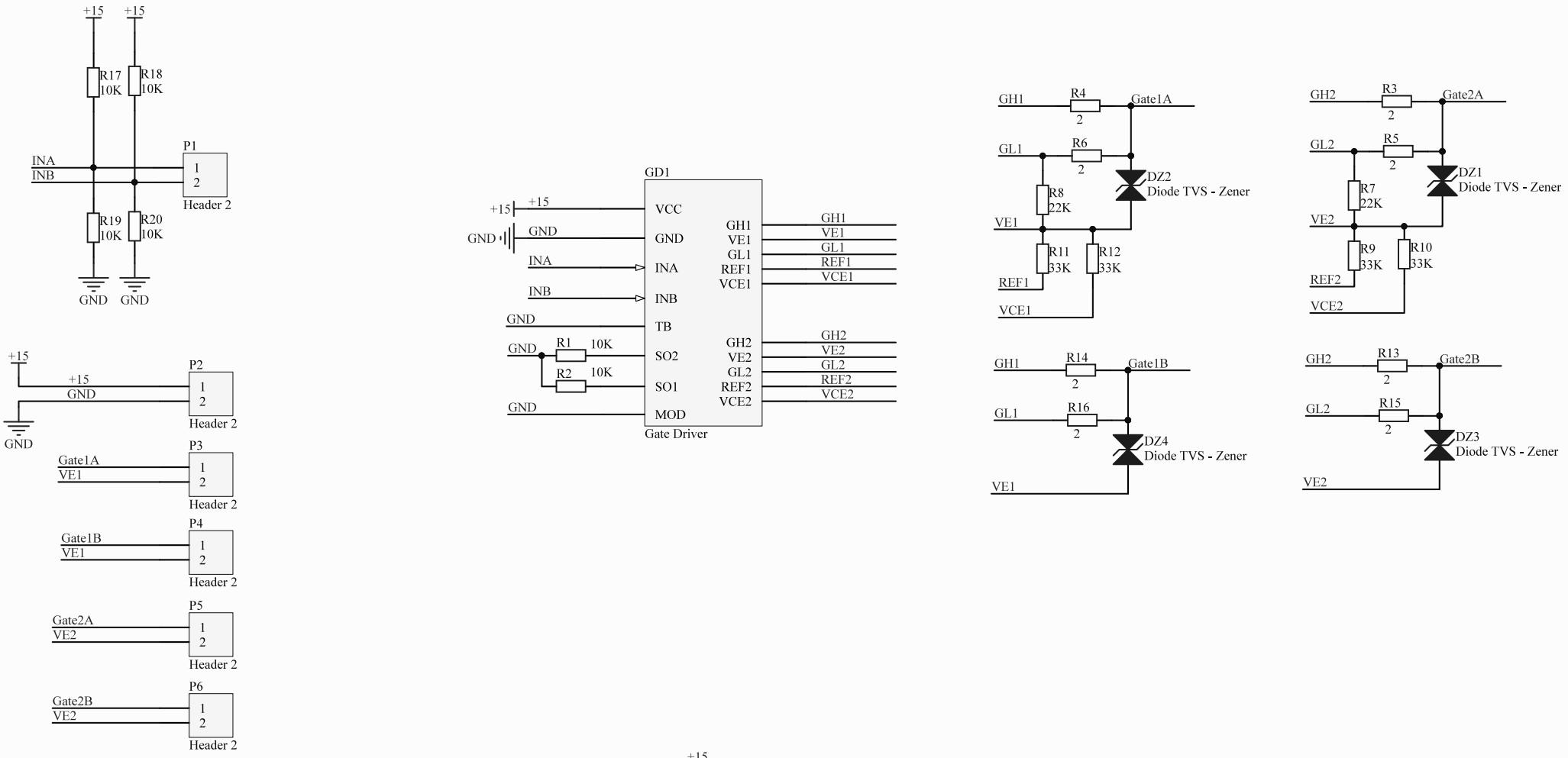
```
257.    InitEPwm1Gpio();        // Inicia configuracoes basicas do modulo 1 do ePWM
258.
259.    EPwm1Regs.ETSEL.bit.SOCAEN      = 1;                    // Enable SOC on A group
260.    EPwm1Regs.ETSEL.bit.SOCASEL     = 4;                    // Select SOC from CMPA on up
    count
261.    EPwm1Regs.ETPS.bit.SOCAPRD      = 1;                    // Generate pulse on 1st even
    t
262.    EPwm1Regs.TBCTL.bit.SYNCOSEL    = TB_SYNC_DISABLE;      //-------------
263.    EPwm1Regs.TBPHS.half.TBPHS      = 1000;
264.    EPwm1Regs.TBCTL.bit.HSPCLKDIV   = TB_DIV1;              // TBCLK = SYSCLK = 90MHz
265.    EPwm1Regs.CMPA.half.CMPA        = 1125;                 // Set compare A value
266.    EPwm1Regs.TBPRD                 = 4500;                 // Set period for ePWM6
267.    EPwm1Regs.TBCTL.bit.CTRMODE     = TB_COUNT_UP ;         // count up and start
268.    EPwm1Regs.AQCTLA.bit.ZRO        = AQ_CLEAR;             // CLEAR at Zero
269.    EPwm1Regs.AQCTLA.bit.CAU        = AQ_SET;               // SET at CompA
270.}
271.
272.
273.void configPWM(void){
274.
275.
276.    // PWM 2
277.
278.    EPwm2Regs.TBPRD =  ts; // Period = 2250 TBCLK counts
279.    EPwm2Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
280.    EPwm2Regs.TBCTL.bit.HSPCLKDIV = 0;
281.    EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Sawtooth
282.    EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
283.    EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
284.    EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO; // sync flow-through
285.    EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
286.    EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
287.    EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
288.    EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
289.    EPwm2Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM2A
290.    EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
291.    EPwm2Regs.AQCTLB.bit.ZRO = AQ_SET; // set actions for EPWM2B
292.    EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
293.
294.    // PWM3
295.
296.    EPwm3Regs.TBPRD =  ts; // Period = 2250 TBCLK counts
297.    EPwm3Regs.TBPHS.half.TBPHS = 0; // Set Phase register to ts/2
298.    EPwm3Regs.TBCTL.bit.HSPCLKDIV = 0;
299.    EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Sawtooth
300.    EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
301.    EPwm3Regs.TBCTL.bit.PRDLD = TB_SHADOW;
302.    EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
303.    EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
304.    EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
305.    EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
306.    EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
307.    EPwm3Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM3A
308.    EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
309.    EPwm3Regs.AQCTLB.bit.ZRO = AQ_SET; // set actions for EPWM3B
310.    EPwm3Regs.AQCTLB.bit.CBU = AQ_CLEAR;
311.
312.    // PWM4
313.
314.    EPwm4Regs.TBPRD =  ts; // Period = 2250 TBCLK counts
315.    EPwm4Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
316.    EPwm4Regs.TBCTL.bit.HSPCLKDIV = 0;
317.    EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Sawtooth
318.    EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
319.    EPwm4Regs.TBCTL.bit.PRDLD = TB_SHADOW;
320.    EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
```

```
321.     EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
322.     EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
323.     EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
324.     EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
325.     EPwm4Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM4A
326.     EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;
327.     EPwm4Regs.AQCTLB.bit.ZRO = AQ_SET; // set actions for EPWM4B
328.     EPwm4Regs.AQCTLB.bit.CBU = AQ_CLEAR;
329.
330.     // PWM5
331.
332.     EPwm5Regs.TBPRD =  ts; // Period = 2250 TBCLK counts
333.     EPwm5Regs.TBPHS.half.TBPHS = ph; // Set Phase register to zero
334.     EPwm5Regs.TBCTL.bit.HSPCLKDIV = 0;
335.     EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Sawtooth
336.     EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
337.     EPwm5Regs.TBCTL.bit.PRDLD = TB_SHADOW;
338.     EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
339.     EPwm5Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
340.     EPwm5Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
341.     EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
342.     EPwm5Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
343.     EPwm5Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM4A
344.     EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR;
345.     EPwm5Regs.AQCTLB.bit.ZRO = AQ_SET; // set actions for EPWM4B
346.     EPwm5Regs.AQCTLB.bit.CBU = AQ_CLEAR;
347.
348.
349.     // PWM6
350.
351.     EPwm6Regs.TBPRD =  ts; // Period = 2250 TBCLK counts
352.     EPwm6Regs.TBPHS.half.TBPHS = ph; // Set Phase register to zero
353.     EPwm6Regs.TBCTL.bit.HSPCLKDIV = 0;
354.     EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Sawtooth
355.     EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
356.     EPwm6Regs.TBCTL.bit.PRDLD = TB_SHADOW;
357.     EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
358.     EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
359.     EPwm6Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
360.     EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
361.     EPwm6Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
362.     EPwm6Regs.AQCTLA.bit.ZRO = AQ_SET; // set actions for EPWM4A
363.     EPwm6Regs.AQCTLA.bit.CAU = AQ_CLEAR;
364.     EPwm6Regs.AQCTLB.bit.ZRO = AQ_SET; // set actions for EPWM4B
365.     EPwm6Regs.AQCTLB.bit.CBU = AQ_CLEAR;
366.
367.
368.     InitEPwm();          // Inicializa o PWM
369.//   InitEPwm1Gpio();     // Default setting for PWM module 1
370.     InitEPwm2Gpio();     // Default setting for PWM module 3
371.     InitEPwm3Gpio();     // Default setting for PWM module 1
372.     InitEPwm4Gpio();     // Default setting for PWM module 1
373.     InitEPwm5Gpio();     // Default setting for PWM module 1
374.     InitEPwm6Gpio();     // Default setting for PWM module 1
375.
376.}
```

ANNEX C – SCHEMATICS


DSP1A
P1
A1 3.3V
A5 GPIO12
A7 GPIO18
A8 GPIO22
A9 GPIO33
A10 GPIO32
TMS320f28069
DSP1B
P2
B1 GND
B2 GPIO19
B3 GPIO44
B5 GPIO16
B10 GPIO55
TMS320f28069
DSP1C
P3
C1 5V
C2 GND
C3 ADCINA7
C4 ADCINB1
C5 ADCINA2
C6 ADCINB2
C7 ADCINA0
C8 ADCINB0
C9 ADCINA1
TMS320f28069
DSP1D
P4
D1 PWM1A
D2 PWM1B
D3 PWM2A
D4 PWM2B
D5 PWM3A
D6 PWM3B
D7 GPIO13
TMS320f28069
DSP1E
P5
E1 3.3V
E5 GPIO20
E7 GPIO14
E8 GPIO21
E9 GPIO23
E10 GPIO54
TMS320f28069
DSP1F
P6
F1 GND
F2 GPIO27
F3 GPIO26
F5 GPIO24
F6 GPIO25
F7 GPIO52
F8 GPIO53
F9 GPIO56
TMS320f28069
DSP1G
P7
G1 5V
G2 GND
G3 ADCINB7
G4 ADCINB4
G5 ADCINA5
G6 ADCINB5
G7 ADCINA3
G8 ADCINB3
G9 ADCINA4
TMS320f28069
DSP1H
P8
H1 PWM4A
H2 PWM4B
H3 PWM5A
H4 PWM5B
H5 PWM6A
H6 PWM6B
TMS320f28069
P2
5V
GND
C17 100 nF
C19 100 nF
C20 100 nF
U13A
U13B
U13C
U13D
U13E
U13F
U14A
U14B
U14C
U14D
U14E
U14F
SN7407
R49
R50
R51
R52
R53
R54
R55
R56
R57
R58
R59
R60
R61
R62
R63
R64
R65
R66
R67
R68
R69
R70
R71
R72
P14 Molex3 PWM12 PWM11
P15 Molex3 PWM10 PWM9
P16 Molex3 PWM8 PWM7
P17 Molex3 PWM6 PWM5
P18 Molex3 PWM4 PWM3
P19 Molex3 PWM2 PWM1
P20 Molex
S1
S2
S3
push-button
R80
R81
R82
GPIO20
GPIO21
GPIO23
C35 10uF
C36 10uF
C37 10uF
C38 10uF
C39 10uF
C40 10uF
C34 100 nF
C33 100 nF
C32 100 nF
C31 100 nF
U12
IN
OUT
C27 100uF
C28 100 nF
C29 100 nF
C30 100uF
DLED5
DLED6
R100
R111
DLED1
DLED2
DLED3
U15F
U15E
U15D
R73
R74
R75
R76
R77
R78
GPIO56
GPIO53
GPIO52


P6
Molex
RDV1
7.5k
RM1
180
GND
5V
U1A
RF1
7.5k
RF2
15k
U1B
ADCINA7
CF1
1nF
100nF
CF2
U9A
TL7726
P7
RDV2
22
CF?
22uF
U2A
RF3
0
RF4
22
U2B
ADCINB1
CF3
22uF
NM
CF4
U9B
TL7726
P8
RDV3
RM3
U3A
RF5
RF6
U3B
ADCINA2
CF5
CF6
100nF
U9C
P9
RDV4
U4A
RF7
RF8
U4B
ADCINA1
CF7
CF8
U9D
P10
RDV5
RM5
U5A
RF9
RF10
U5B
ADCINB0
CF9
CF10
U10A
P11
RDV6
RM6
U6A
RF11
RF12
U6B
ADCINA0
CF11
CF12
U10B
P12
RDV7
CF?
1nF
U7A
RF13
RF14
U7B
ADCINB2
CF13
22uF
NM
U10C
P13
RDV8
RM8
U8A
RF15
RF16
U8B
ADCINB7
CF15
1nF
CF16
U10D
U9G
U10G
3.3V
C51
C52
C9
C10
C11
C12
C13
C14
C15
C16
C41
47uF
C42
C44
C45
C46
C47
C48
C43
C49
C50
100 nF


+15
+15
R17
10K
R18
10K
INA
INB
P1
1
2
Header 2
R19
10K
R20
10K
GND
GND
GD1
+15
GND
INA
INB
GND
GND
R1
10K
R2
10K
GND
VCC
GND
INA
INB
TB
SO2
SO1
MOD
GH1
VE1
GL1
REF1
VCE1
GH2
VE2
GL2
REF2
VCE2
Gate Driver
GH1
R4
2
Gate1A
GL1
R6
2
DZ2
Diode TVS - Zener
R8
22K
VE1
R11
33K
R12
33K
REF1
VCE1
GH2
R3
2
Gate2A
GL2
R5
2
DZ1
Diode TVS - Zener
R7
22K
VE2
R9
33K
R10
33K
REF2
VCE2
+15
+15
GND
GND
P2
1
2
Header 2
Gate1A
VE1
P3
1
2
Header 2
Gate1B
VE1
P4
1
2
Header 2
Gate2A
VE2
P5
1
2
Header 2
Gate2B
VE2
P6
1
2
Header 2
GH1
R14
2
Gate1B
GL1
R16
2
DZ4
Diode TVS - Zener
VE1
GH2
R13
2
Gate2B
GL2
R15
2
DZ3
Diode TVS - Zener
VE2
+15
C1
Cap Pol3
100pF
C2
Cap
100pF
C3
Cap
100pF
C4
Cap
100pF
C5
Cap
100pF
GND

ANNEX D – LIST OF COMPONENTS

COMPONENT	DESCRIPTION	MANUFACTURER	PART NUMBER
IGBT And Diode	IGBT Module Trench Single 1200V 187A 890W	VISHAY	VS-GT100DA120UF
Capacitor	CAP ALUM 2400UF 20% 450V SCREW	KEMET	ALS70A242KF450
Voltage Sensor	TRANSDUCR VOLTAG CLOSE LOOP 10mA	LEM	LV 25-P/SP5
Current Sensor	SENSOR CURRENT HALL 100A AC/DC	LEM	HASS 100-S
DSP	LAUNCH PAD PICCOLO C2000 LAUNCHXL-F28069M	TEXAS INSTRUMENTS	LAUNCHXL-F28069M
Heatsink	Rth = 0.1 °C/W @ 10 m/s forced air	(LOCAL SUPPLIER)	-
Gate Driver	IC DUAL GATE DRIVER 8A	Power Integrations	2SC0108T2D0-12
Fan	FAN AXIAL 120X38MM 12VDC WIRE	NMB Technologies Corporation	4715VL-04W-B80-E00
Main Inductor Core	Mn-Zn EE Ferrite Core	Thornton	EE 76/50/76
Auxiliary Power Supply	AC/DC CONVERTER 5V +/-15V 66W RT-65C	MEAN WELL USA Inc.	RT-65C