# Method for Deriving Transformerless Common-Ground Voltage Source Inverter Topologies

Gabriel de O. Assunção, *Student Member, IEEE*, and Ivo Barbi, *Life Fellow, IEEE*

***Abstract*—This article presents a method for generating a family of transformerless inverters with common ground, for the connection of photovoltaic or battery energy storage systems with the electrical grid. Using the proposed method, four common-ground buck type inverter topologies are derived from bidirectional dc–dc converters based on buck–boost, SEPIC, zeta and boost–buck converters, which have in common the static gain given by $D/(1-D)$. The operation of each generated topology is explained and confirmed by computer simulation results. A comparative analysis between the four generated topologies and other transformerless common-ground inverters are included, considering the number of components, voltage ratings, output power, switching frequency, reported efficiency at rated power, and the requirement for filter insertion. Experimental results obtained in the laboratory, with tests performed on a nonoptimized experimental prototype are presented, for the topology based on the bidirectional zeta converter.**

***Index Terms*—Common-ground inverter, grid-tied inverter, inverter topologies, leakage current, transformerless inverter.**

## I. Introduction

WITH more than 200 GW of installed capacity added to the power sector in 2019, renewable energy continues for five consecutive years to outpace the additions of fossil fuel and nuclear power installations combined. About 115 GW of this total came from photovoltaic solar energy alone [1].

In addition, new distributed systems were motivated by self-consumption, increasingly with energy storage. In the United States, particularly Hawaii, and California, where consumers are looking for energy resilience and reliability, interest in solar PV-plus-storage projects is also increasing in the residential market [1].

The use of inverters without galvanic isolation in the connection of photovoltaic and energy storage systems with the electrical grid can contribute to cost reduction and increase the efficiency of these systems. However, the use of conventional noninsulated converters is not suitable due to the generation floating voltage, which cause the circulation of leakage currents through the parasitic capacitors [2], [3].

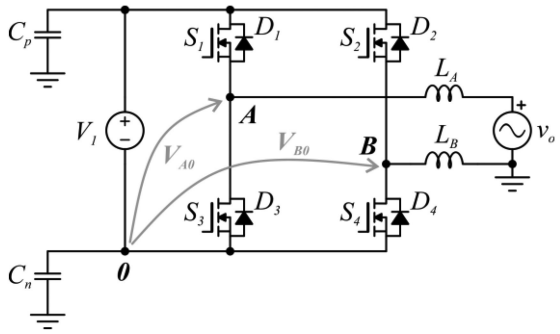



Fig. 1. Classic full-bridge voltage source inverter used to connect a dc power source to the grid.

As follows from the classic full bridge voltage source inverter shown in Fig. 1, the voltage between the dc and the ac link depends on the voltages $V_{A0}$, and $V_{B0}$ across the power semiconductors. Therefore, the dc link voltage is floating with respect to the grounded point.

In [2] and [3], this effect is analyzed mathematically, and it is demonstrated how the switching strategy of the power semiconductor affects this floating voltage, also called the common mode voltage. Thus, through stray capacitances, present in photovoltaic and energy storage systems [4], [5], an unwanted current flows through the ground, generating problems such as risk of electric shock, reduction in the quality of the generated energy, appearance of electromagnetic interference, increases in total harmonic distortion (THD) and power losses, and possible occurrence of a trip in the earth fault protection devices [3], [6], [7].

Thus, seeking to solve the problems caused by the floating voltage, while maintaining the advantages of a transformerless inverter, several topologies were proposed [8].

The first transformerless inverters proposed for PV applications were based on classic inverters: full-bridge (H4) and neutral point clamped (NPC) [9]. The H5 [10], the H6 [11], and the HERIC [12] can be mentioned as full-bridge inverter derivations.

Manuscript received June 7, 2021; revised September 29, 2021 and January 4, 2022; accepted March 11, 2022. Date of publication March 28, 2022; date of current version May 23, 2022. This work was supported by CAPESBrazilian Federal Agency for Support and Evaluation of Graduate Education within the Ministry of Education of Brazil under Grant 88882.344611/2019-01, and by the Federal University of Santa Catarina. Recommended for publication by Associate Editor G. Moschopoulos. *(Corresponding author: Gabriel de O. Assunção.)*

The authors are with the Department of Electrical and Electronics Engineering, Federal University of Santa Catarina, Florianopolis 88040-900, Brazil (e-mail: gabriel.oassuncao@gmail.com; ivobarbi@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3162771.

Digital Object Identifier 10.1109/TPEL.2022.3162771

0885-8993 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

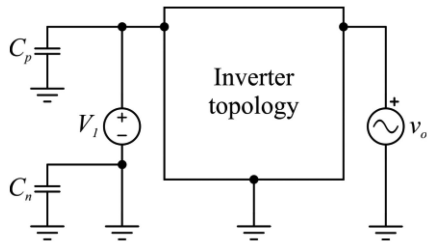



Fig. 2. Common-ground inverter principle.

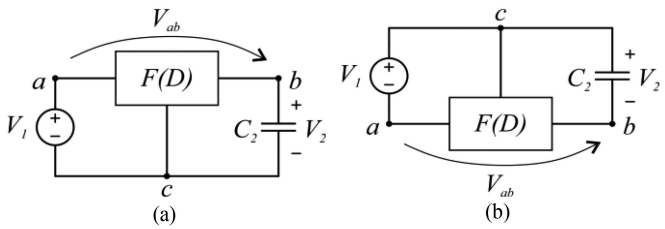



Fig. 3. Nonisolated bidirectional dc–dc converter with (a) common connection of negative terminals, and (b) common connection of positive terminals.

Conergy NPC [13] and active NPC [14] are modifications of the NPC converter.

However, in addition to these two lines of topology derivation, some converters connecting the grid neutral point to the negative dc terminal have been proposed [15]–[19]. Therefore, these three strategies lead transformerless inverter structures to be categorized as: disconnection during the freewheeling modes, common-mode voltage clamping, or common-ground [6].

Among the strategies used to solve the leakage current problem, the topologies with common grounding gained prominence for being the only one that eliminates this current [18]–[23]. This is achieved because the principle of this strategy is to have a direct physical connection point between the ac and dc links, commonly connecting the grid neutral point to the negative dc source, as shown in Fig. 2.

Some of the common-ground topologies were developed from known converters [24]. However, based on a literature search, a systematic method for derivation of common-ground voltage source inverters does not appear to have been previously reported. Nevertheless, systematic procedures for generating floating voltage step-down inverter topologies are presented in [25], and a derivation method for avoiding floating operations in ac-based decoupling topologies is presented in [26].

Therefore, a method for generating inverters with common ground is proposed in this article, which can be used to generate a large number of inverter topologies, from bidirectional dc–dc converters, suitable for connecting photovoltaic and energy storage systems to the electrical power grid.

## II. Bidirectional Nonisolated DC–DC Converters

Fig. 3(a) shows a generic nonisolated bidirectional dc–dc converter represented by $F(D)$, interconnecting a voltage source $V_1$ and a capacitor $C_2$, with common connection between the negative polarity terminals. Fig. 3(b) shows the same converter,

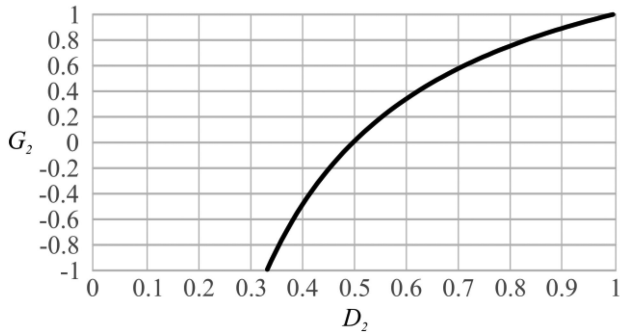



Fig. 4. Static gain $G_2$ as a function of $D_2$.

but with a common connection between the positive terminals of the source $V_1$ and the capacitor $C_2$.

Let us consider the connection of the positive terminals. The voltages shown in Fig. 3(b) are described by

$$V_2 = F(D)V_1 \tag{1}$$

$$V_{ab} + V_2 = V_1 \tag{2}$$

where $F(D)$ is a function of duty cycle, which depends on the topology of the converter. Substituting (1) in (2), we obtain

$$V_{ab} = V_1 - F(D)V_1 = V_1\left[1 - F(D)\right]. \tag{3}$$

Hence, the dc voltage conversion ratio is

$$G = \frac{V_{ab}}{V_1} = 1 - F(D). \tag{4}$$

Therefore, the voltage gain is positive when $F(D) < 1$ and negative when $F(D) > 1$. Let us assume that $F(D)$ it is given by

$$F(D_1) = \frac{D_1}{1 - D_1} \tag{5}$$

where $D_1$ is the duty cycle. Hence, the complementary duty cycle is

$$D_2 = 1 - D_1. \tag{6}$$

Thus,

$$F(D_2) = \frac{1 - D_2}{D_2}. \tag{7}$$

Substituting (5) or (7) in (4), we obtain

$$G_1 = 1 - \frac{D_1}{1 - D_1} = \frac{1 - 2D_1}{1 - D_1} \tag{8}$$

$$G_2 = 1 - \frac{1 - D_2}{D_2} = \frac{2D_2 - 1}{D_2}. \tag{9}$$

As the gain given by (8) and (9) complementary, we choose to use the gain described by $G_2$, which increases with the duty cycle, according to the curve plotted in Fig. 4.

Equations (4) and (7) and Fig. 4 show that the voltage can have positive or negative values with respect to the input voltage, depending on the value of the duty cycle. Hence, we can write

$$\begin{cases} 0 \le G \le 1 \rightarrow D \ge 0.5 \\ G < 0 \rightarrow D < 0.5. \end{cases} \tag{10}$$

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

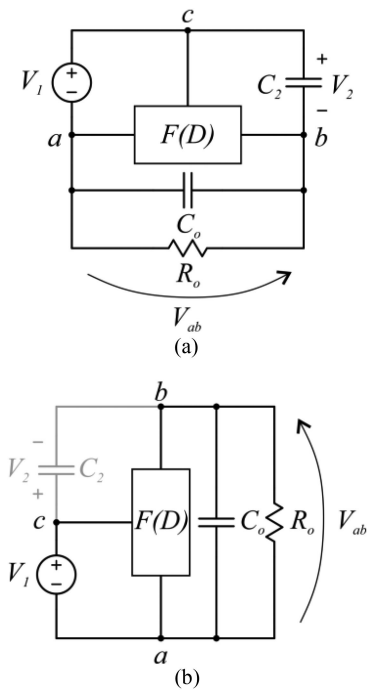



Fig. 5. (a) Circuit shown in Fig. 3(b) with the pair *RC* added at the terminals *ab*. (b) Same circuit, redraw without the capacitor $C_2$.

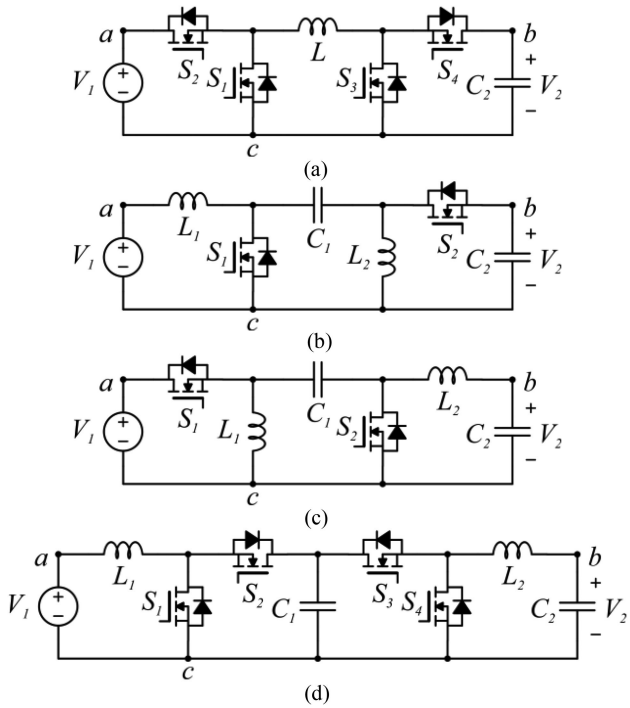



Fig. 6. Common negative connection in the bidirectional dc–dc converters. (a) Buck–boost with positive output. (b) SEPIC. (c) Zeta. (d) Boost–buck.

It is possible to add a pair *RC* at the terminals *ab* without modifying the operating principles, as shown in Fig. 5(a). By redrawing the circuit, we can obtain the form shown in Fig. 5(b), suggesting that the voltage $V_{ab}$ at the load, with a common connection point with the input voltage source $V_1$, can be alternating, provided that the duty cycle be properly controlled.

The quasi-instantaneous average voltages across capacitors $C_2$ and $C_o$ do not depend of the presence of $C_2$. Therefore, it is redundant and can be excluded from the circuit. The consequence of this is just an increase in the high frequency component of the current in the capacitor $C_o$.

This result suggests a generic methodology for deriving voltage source inverter topologies with common ground between the input power supply and one of the load voltage terminals, employing bidirectional dc–dc converters regardless of their topology, as long as their static characteristic can be given by (5).

## III. Derivation of a Family of Voltage Source Common-Ground Inverters

Let us consider the four nonisolated bidirectional dc–dc converters shown in Fig. 6, which are: 1) buck–boost converter with positive output, shown in Fig. 6(a), 2) SEPIC converter, shown in Fig. 6(b), 3) zeta converter, shown in Fig. 6(c), and 4) boost–buck converter, shown in Fig. 6(d). In all topologies, there is a common connection between the negative terminals of the input and output voltage sources. The same topologies are shown in Fig. 7, but with common connections between the positive terminals of the input and output voltage sources.

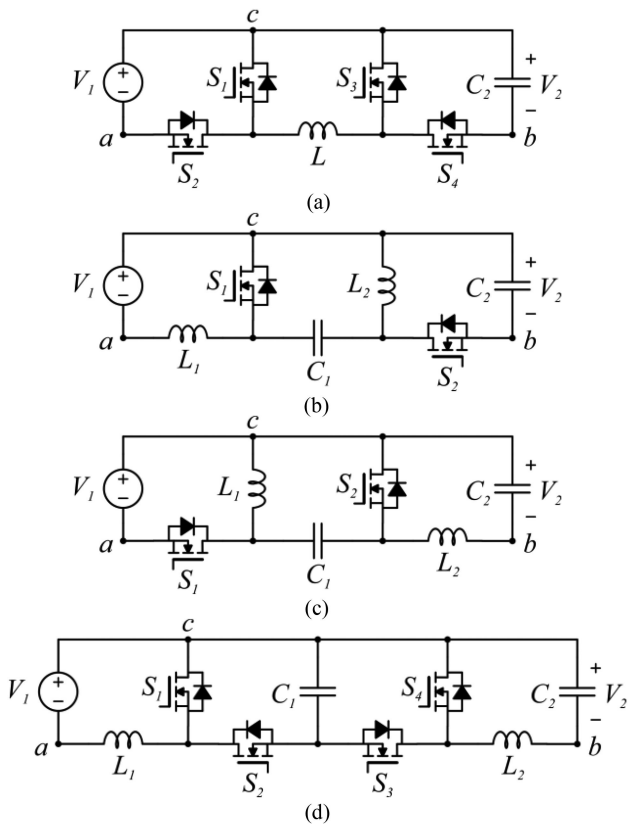



Fig. 7. Common positive connection in the bidirectional dc–dc converters. (a) Buck–boost with positive output. (b) SEPIC. (c) Zeta. (d) Boost–buck.

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

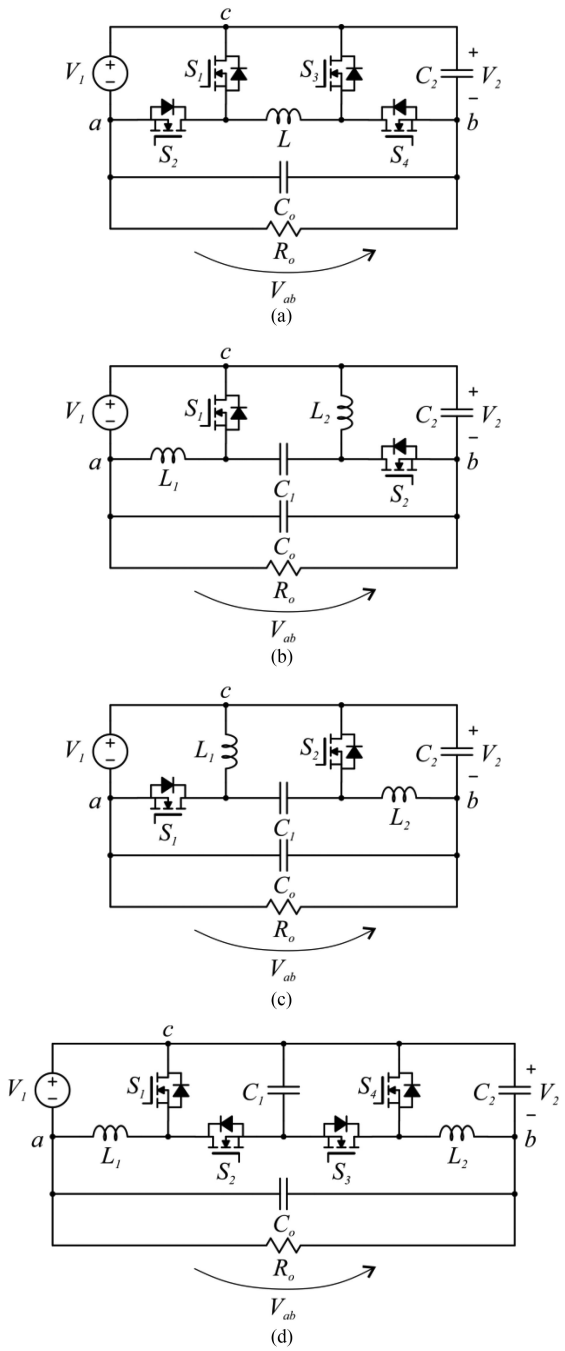



Fig. 8. Adding a *RC* load to the: (a) bidirectional buck–boost with positive output, (b) bidirectional SEPIC, (c) bidirectional zeta, and (d) bidirectional boost–buck.

Fig. 8 shows the same topologies of Fig. 7, in the same order, but with the pairs $R_oC_o$, which represent the load, connected at terminals *ab*.

By properly redrawing the topologies shown in Fig. 8, the common ground voltage source inverter topologies shown in Fig. 9 are obtained, generated by (a) the nonisolated buck–boost with positive output, (b) SEPIC, (c) zeta, and (d) boost–buck bidirectional converters. In all cases, the capacitor $C_2$, being redundant, was removed from the circuit.

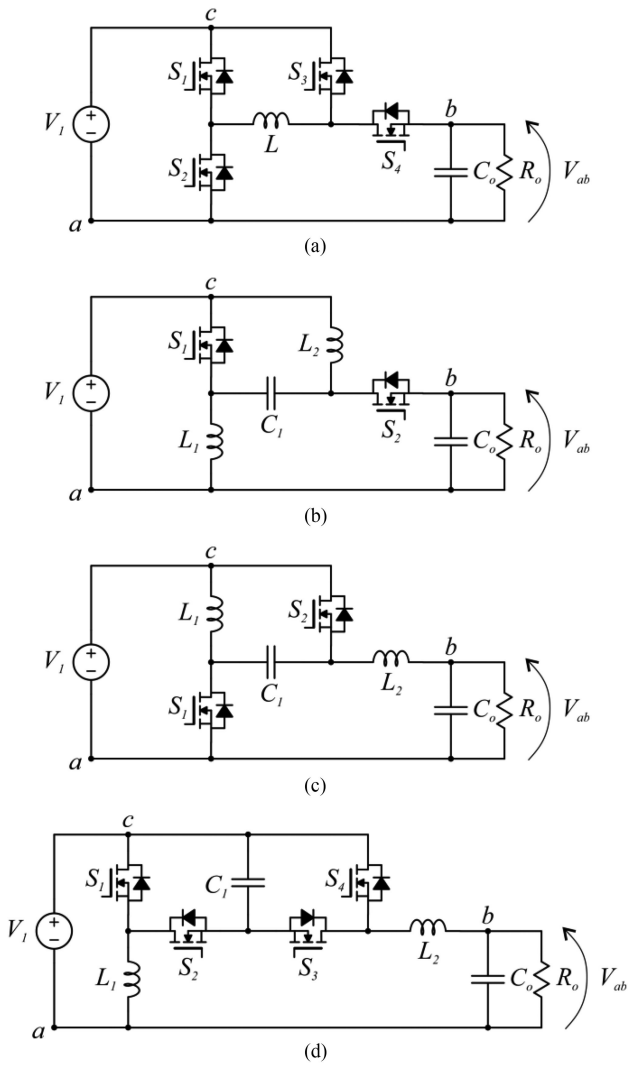



Fig. 9. Transformerless common-ground inverters derived from: (a) bidirectional buck–boost with positive output, (b) bidirectional SEPIC, (c) bidirectional zeta, and (d) bidirectional boost–buck converters.

The topologies shown in Fig. 9(b) and (c) were originally published by Cao *et al.* [27], and were respectively designated semi-Z-source and semi-quasi-Z-source inverters. In the article, however, a systematic method for obtaining the topologies is not presented. The semi-quasi-Z-source inverter was also studied in [27] and [28] with the inclusion of control strategy and experimental results.

## IV. Operating Principles

As the converters necessarily operate in continuous conduction mode, for each of them there are two topological states in a switching period. The gate signals are indicated in Table I, where $v_{g1}$ defines the duty cycle $D$ while $v_{g2}$ defines the complementary duty cycle $1 - D$.

For the analysis, a switching period where the output voltage is positive is considered. The topological states of each inverter are shown in Fig. 10. The corresponding and relevant waveforms for all topologies are shown in detail in Fig. 11.

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

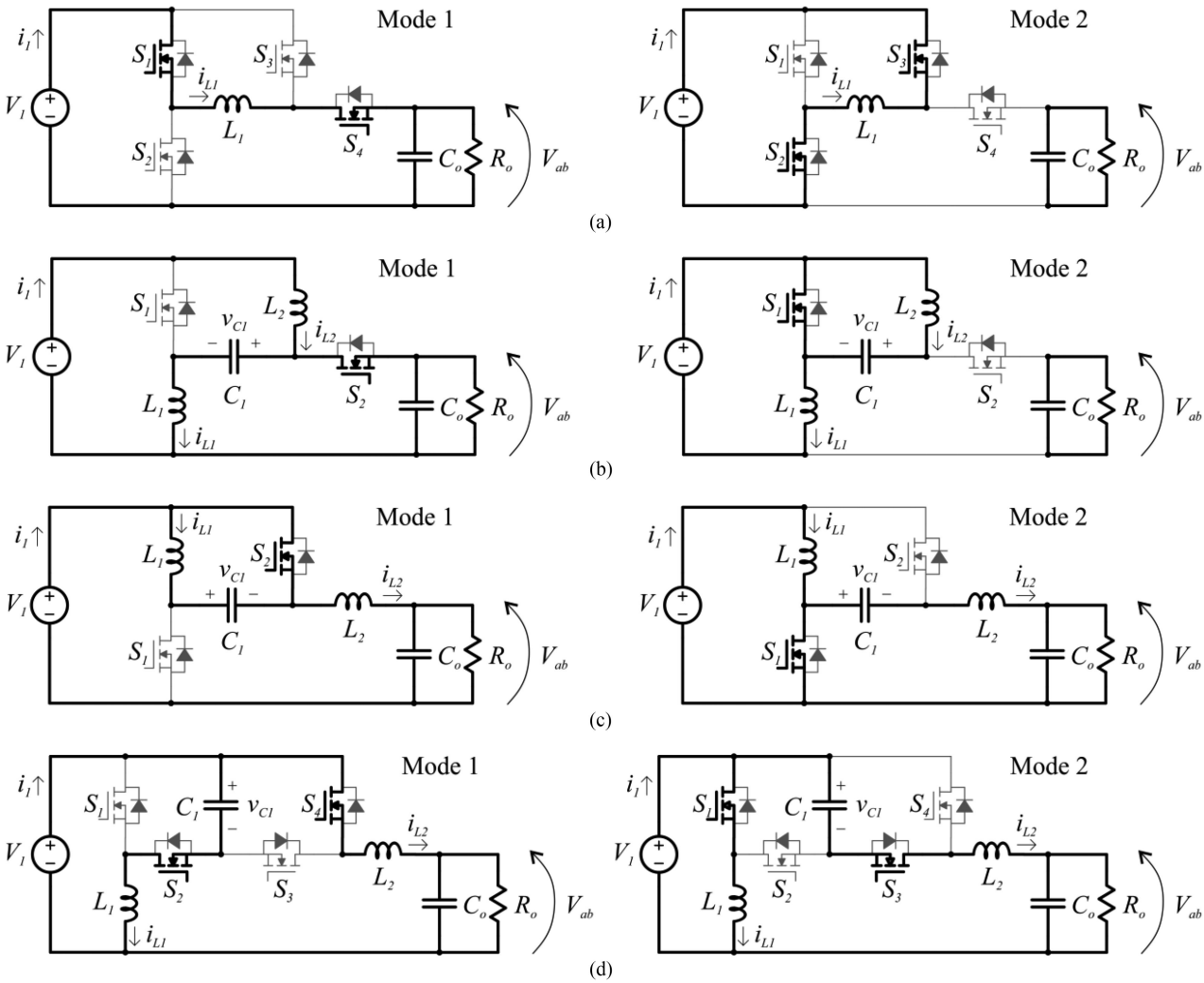



Fig. 10. Topological states for a switching period of the common-ground inverters derived from (a) buck–boost with positive output, (b) SEPIC, (c) zeta, and (d) boost–buck bidirectional dc–dc converters.

TABLE I
GATE SIGNAL IN EACH TOPOLOGY

| Gate Signal | Topology | | | |
|---|---|---|---|---|
| | Buck-Boost | SEPIC | Zeta | Boost-Buck |
| $v_{g1}$ | $S_1$ , $S_4$ | $S_2$ | $S_2$ | $S_2$ , $S_4$ |
| $v_{g2}$ | $S_2$ , $S_3$ | $S_1$ | $S_1$ | $S_1$ , $S_3$ |

From these waveforms, the current and voltage stresses in each topology are obtained. The equations found are summarized in Table II, were

$$x_1 = 6 - 2\alpha^2 + \left(4 - \alpha^2\right)^{3/2} \tag{11}$$

$$x_2 = 4 - \alpha^2 \tag{12}$$

$$x_3 = 2\alpha^4 - 7\alpha^2 + 8 \tag{13}$$

$$x_4 = 2\left(4 - \alpha^2\right)^{5/2} - 6\alpha^4 + 35\alpha^2 - 56 \tag{14}$$

$$x_5 = 3\alpha^4 + 4\alpha^2 + 16 \tag{15}$$

$$x_6 = 8\alpha^4 - 64\alpha^2 + 128. \tag{16}$$

## V. SIMULATION RESULTS

In order to verify the operation of the generated inverters, open loop simulations were carried out, with the specifications shown in Table III. The values of the inductances and capacitances were determined using the equations shown in Table IV and the parameters obtained are presented in Table V.

To obtain an approximately sinusoidal output alternating voltage, without a voltage control loop, a static linearizing function is employed, resulting in a time-varying duty cycle given by

$$D(t) = \frac{1}{2 - \alpha \sin(\omega t)} \tag{17}$$

where $\omega$ is the angular frequency, in radians, of the output alternating voltage, and $\alpha$ is defined by

$$\alpha = \frac{V_{abpk}}{V_1}. \tag{18}$$

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

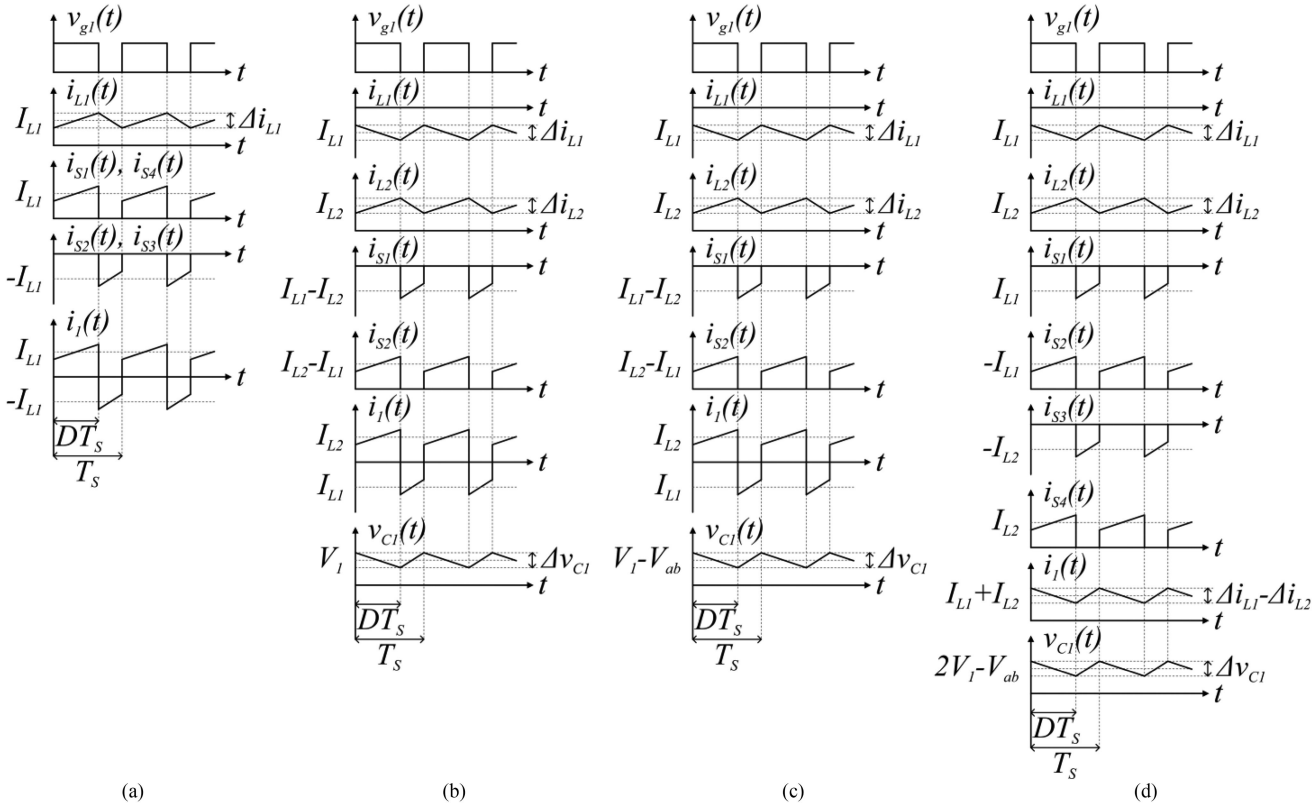



Fig. 11. Typical waveforms of the derived inverters: (a) buck–boost, (b) SEPIC, (c) zeta, and (d) boost–buck.

TABLE II
CURRENT AND VOLTAGE STRESS PER TOPOLOGY

| Variable | Topology | | | |
|---|---|---|---|---|
| | Buck-boost | SEPIC | Zeta | Boost-buck |
| $I_{L1rms}$ | $\sqrt{I_{orms}^2\left(4+\frac{3}{4}\alpha^2\right)+\frac{V_1^2 x_1}{12L_1^2 f_s^2 x_2^{3/2}}}$ | $\sqrt{I_{orms}^2\left(1+\frac{3}{4}\alpha^2\right)+\frac{V_1^2 x_1}{12L_1^2 f_s^2 x_2^{3/2}}}$ | | |
| $I_{L2rms}$ | - | $\sqrt{I_{orms}^2+\frac{V_1^2 x_1}{12L_2^2 f_s^2 x_2^{3/2}}}$ | | |
| $I_{S1rms}$ | $\sqrt{2I_{orms}^2+\frac{V_1^2 x_3}{24L_1^2 f_s^2 x_2^{5/2}}}$ | $\sqrt{I_{orms}^2\left(2+\frac{3}{4}\alpha^2\right)+\frac{V_1^2\left(L_1+L_2\right)^2 x_4}{24L_1^2 L_2^2 f_s^2 x_2^{5/2}}}$ | | $\sqrt{I_{orms}^2\left[\frac{x_5 x_2^{5/2}-32x_2^2}{4\alpha^2 x_2^{5/2}}\right]+\frac{V_1^2 x_4}{24L_1^2 f_s^2 x_2^{5/2}}}$ |
| $I_{S2rms}$ | $\sqrt{I_{orms}^2\left(2+\frac{3}{4}\alpha^2\right)+\frac{V_1^2 x_4}{24L_1^2 f_s^2 x_2^{5/2}}}$ | $\sqrt{2I_{orms}^2+\frac{V_1^2\left(L_1+L_2\right)^2 x_3}{24L_1^2 L_2^2 f_s^2 x_2^{5/2}}}$ | | $\sqrt{I_{orms}^2\left(\frac{x_6-4x_2^{5/2}}{\alpha^2 x_2^{5/2}}\right)+\frac{V_1^2 x_3}{24L_1^2 f_s^2 x_2^{5/2}}}$ |
| $I_{S3rms}$ | $\sqrt{I_{orms}^2\left(2+\frac{3}{4}\alpha^2\right)+\frac{V_1^2 x_4}{24L_1^2 f_s^2 x_2^{5/2}}}$ | - | | $\sqrt{I_{orms}^2\left(\frac{\left(4+\alpha^2\right)x_2^{5/2}-x_6}{\alpha^2 x_2^{5/2}}\right)+\frac{V_1^2 x_4}{24L_2^2 f_s^2 x_2^{5/2}}}$ |
| $I_{S4rms}$ | $\sqrt{2I_{orms}^2+\frac{V_1^2 x_3}{24L_1^2 f_s^2 x_2^{5/2}}}$ | - | | $\sqrt{I_{orms}^2\left(\frac{x_6-4x_2^{5/2}}{\alpha^2 x_2^{5/2}}\right)+\frac{V_1^2 x_3}{24L_2^2 f_s^2 x_2^{5/2}}}$ |
| $I_{C1rms}$ | - | $\sqrt{I_{orms}^2+\frac{V_1^2\left(L_1^2 x_4+L_2^2 x_3\right)}{24L_1^2 L_2^2 f_s^2 x_2^{5/2}}}$ | | |
| $V_{C1pk}$ | - | $V_1$ | $V_1+V_{abpk}$ | $2V_1+V_{abpk}$ |
| $V_{S1max}$ | $V_1$ | $2V_1+V_{abpk}$ | | |
| $V_{S2max}$ | $V_1$ | $2V_1+V_{abpk}$ | | |
| $V_{S3max}$ | $V_1+V_{abpk}$ | - | | $2V_1+V_{abpk}$ |
| $V_{S4max}$ | $V_1+V_{abpk}$ | - | | $2V_1+V_{abpk}$ |

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

TABLE III
DESIGN SPECIFICATIONS

| Symbol | Description | Value |
|---|---|---|
| $V_1$ | DC input voltage | 400 V |
| $V_{abrms}$ | Load voltage (RMS) | 220 V |
| $P_o$ | Output power | 1 kW |
| $f_s$ | Switching frequency | 50 kHz |
| $f_o$ | Output voltage frequency | 60 Hz |
| $\Delta i_{L1\%}$ | Current ripple in $L_1$ | 20% |
| $\Delta i_{L2\%}$ | Current ripple in $L_2$ | 5% |
| $\Delta v_{C1\%}$ | Voltage ripple across $C_1$ | 5% |
| $\Delta v_{Co\%}$ | Voltage ripple across $C_o$ | 1% |

TABLE IV
DESIGN ORIENTED EQUATIONS BY TOPOLOGY

| Element | Topology | | | |
|---|---|---|---|---|
| | Buck-boost | SEPIC | Zeta | Boost-buck |
| $L_1$ | $\frac{V_1}{\Delta i_{L1} f_s}\left(\frac{1+\alpha}{2+\alpha}\right)$ | | | |
| $L_2$ | - | $\frac{V_1}{\Delta i_{L2} f_s}\left(\frac{1+\alpha}{2+\alpha}\right)$ | | |
| $C_1$ | - | $\frac{I_o\sqrt{2}}{\Delta v_{C1} f_s}\left(\frac{1+\alpha}{2+\alpha}\right)$ | | |
| $C_o$ | $\frac{I_o\sqrt{2}}{\Delta v_{Co} f_s}\left(\frac{1+\alpha}{2+\alpha}\right)$ | | $\frac{\Delta i_{L2}}{2\pi f_s \Delta v_{Co}}$ | |

TABLE V
PASSIVE COMPONENTS OF EACH INVERTER

| Element | Topology | | | |
|---|---|---|---|---|
| | Buck-boost | SEPIC | Zeta | Boost-buck |
| $L_1$ | 1.43 mH | 10.24 mH | 10.24 mH | 10.24 mH |
| $L_2$ | - | 15.93 mH | 15.93 mH | 15.93 mH |
| $C_1$ | - | 4.11 µF | 2.31 µF | 1.48 µF |
| $C_o$ | 26.45 µF | 26.45 µF | 328.83 nF | 328.83 nF |
| $R_o$ | 48.4 Ω | | | |

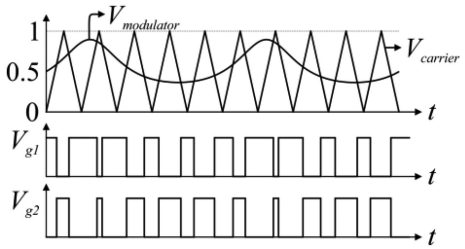



Fig. 12. Bipolar PWM modulator signals applied to generate the power semiconductor gate signals of all inverter topologies generated.

The classic bipolar modulator is employed to generate the power semiconductor gate signals of all proposed inverters, which relevant signals are shown in Fig. 12. It is the same modulation strategy used in conventional half-bridge inverters, in which the modulating signal is generated by the current controller.

The output voltage of each inverter can be seen in Fig. 13. In this same figure, the output voltage of the conventional full-bridge inverter is added to be a comparative parameter

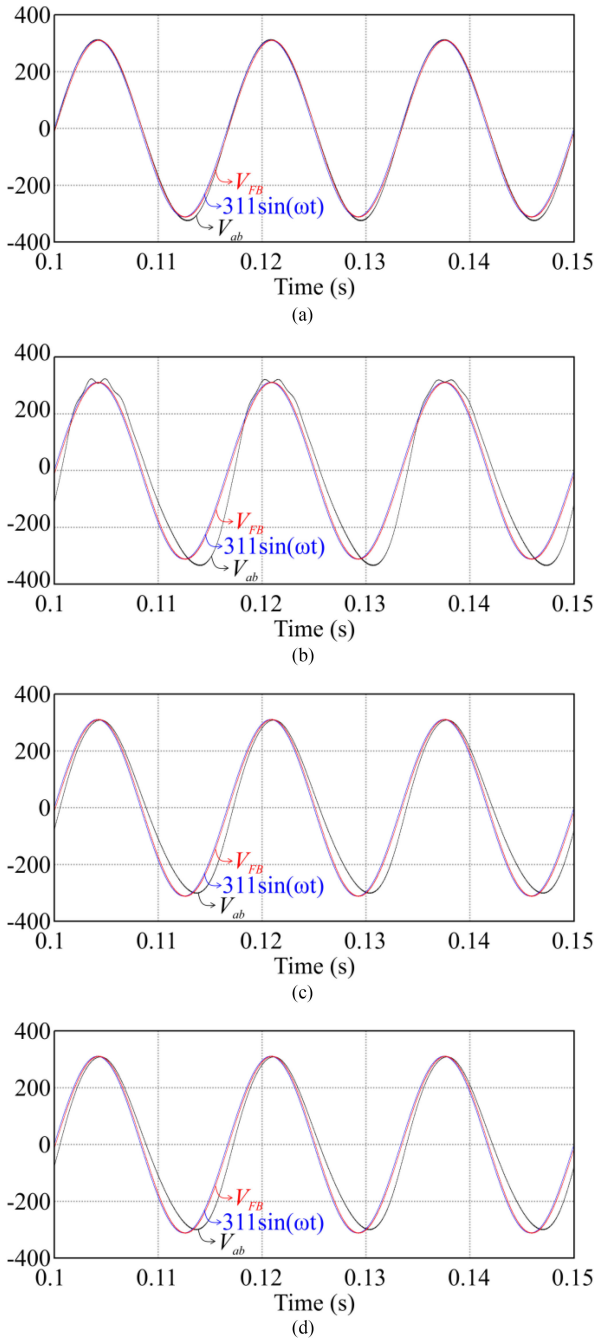



Fig. 13. Output voltage of the derived inverters compared to the output voltage of the full-bridge inverter, both without closed-loop control: (a) buck–boost, (b) SEPIC, (c) zeta, and (d) boost–buck.

of the conventional topology. It is designed for the same parameters shown in Table III, resulting in a 6.22 mH inductor and a 328.83 nF capacitor. The small distortions and delays observed in the output voltage in relation to the sinusoidal reference voltage can be eliminated or minimized with the use of closed-loop voltage control.

## VI. EXPERIMENTAL RESULTS

In order to validate the presented method for generating the inverter family topologies, a nonoptimized prototype of the

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

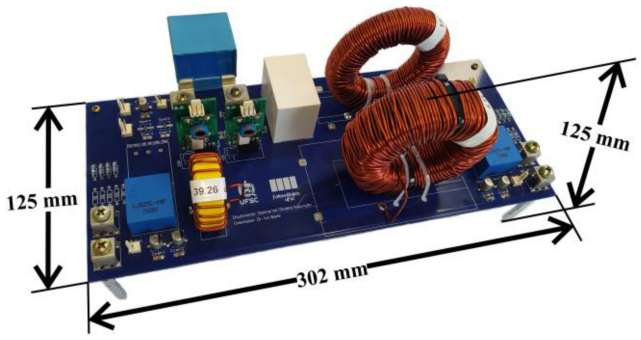



Fig. 14. Photograph of the experimental prototype based on the zeta converter.

TABLE VI
EXPERIMENTAL PROTOTYPE COMPONENTS

| Component | Specification |
|---|---|
| Inductor $L_1$ | Inductance: 4.13 mH |
| | Number of turns: 173 |
| | Wire: 1 x 15 AWG |
| | Core: 2 x MMTS60T7713 (Magmattec) |
| Inductor $L_2$ | Inductance: 1.60 mH |
| | Number of turns: 152 |
| | Wire: 1 x 15 AWG |
| | Core: 1 x MMTS60T7713 (Magmattec) |
| Inductor $L_f$ | Inductance: 39.26 µH |
| | Number of turns: 19 |
| | Wire: 1 x 15 AWG |
| | Core: 1 x MMT026T4015 (Magmattec) |
| Capacitor $C_1$ | 2 µF (2 x 1 µF/1.25 kV - B32656S7105K577) |
| Capacitor $C_f$ | 30 µF/650 V - C4AQCBW5300A3JJ |
| Capacitor $C_o$ | 1 µF/630 V |
| Switches $S_1$ and $S_2$ | C2M0080170P (1700 V/40 A) |
| Heatsink | LAM 3 K 150 12 (Fischer Elektronik) |

inverter generated by the zeta bidirectional dc–dc converter was designed and built, as shown in Fig. 14. The specifications are shown in Table III, however with current ripple in $L_1$ and $L_2$ equal to 50%, and voltage ripple across $C_o$ equal to 3%. The components are given in Table VI. To eliminate the high frequency in the input current, an $LC$ filter composed of $L_f$ and $C_f$ was utilized between the input voltage source and the inverter power stage.

The experimentation was carried out with the inverter operating in open loop for three different loads as follows: 1) purely resistive load with R = 47 Ω, 2) resistive-inductive load with R = 16.5 Ω and L = 120.8 mH, and 3) resistive-capacitive load with R = 35 Ω and C = 72 $\mu$F, with modulating signal according to (17), which includes the static linearizing function.

Input and output voltages and currents are shown in Fig. 15 for each case. Note that the experimental load voltage is similar to the simulation results. The voltage THD of 3.96% was measured using a Tektronix PA4000 power analyzer for the purely resistive load. Resistive-inductive and resistive-capacitive loads change the value of this THD to 7.53% and 4.49%, respectively. However, these distortions can be eliminated or reduced by implementing a closed-loop voltage control.

The voltage ripples across capacitors $C_1$, $C_f$, and $C_o$ are shown in Fig. 16. The measured peak-to-peak values were 32 V and 12 V for $\Delta v_{C1}$ and $\Delta v_{Co}$, respectively.

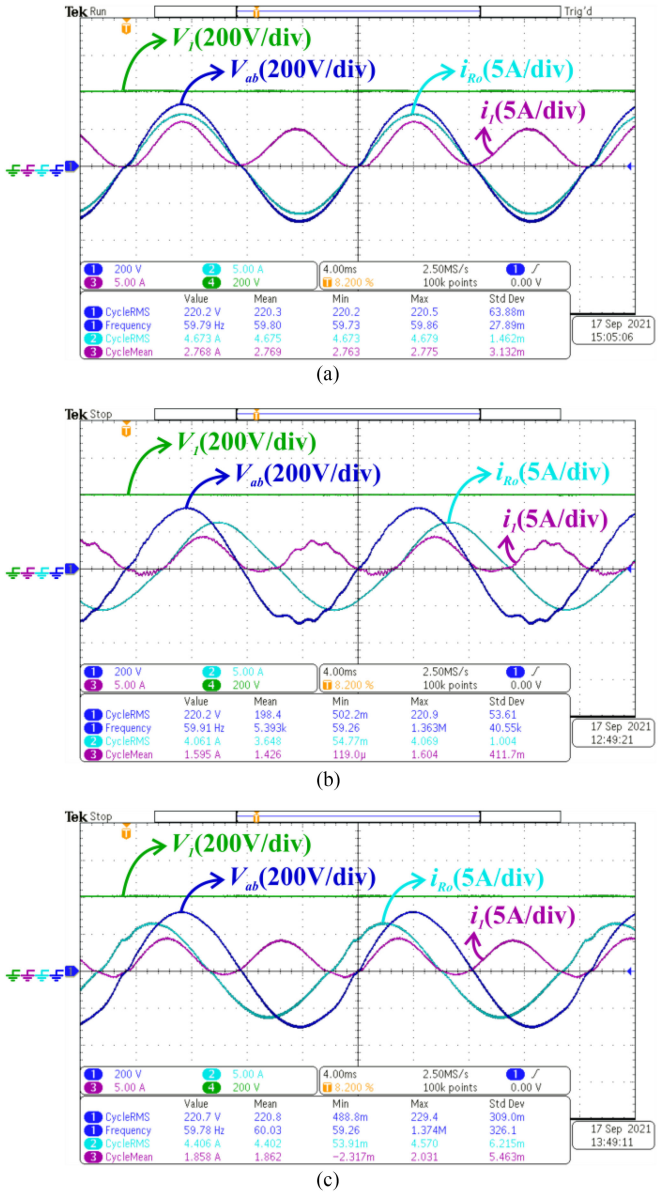



Fig. 15. Experimental input and output voltages and currents for (a) resistive, (b) resistive inductive, and (c) resistive-capacitive loads.

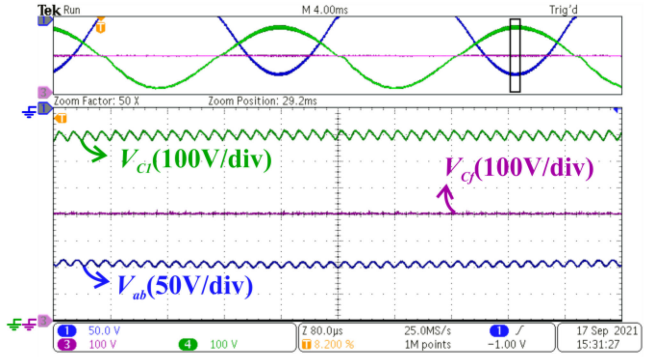



Fig. 16. Experimental voltage ripple across capacitors $C_1$, $C_f$, and $C_o$.

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

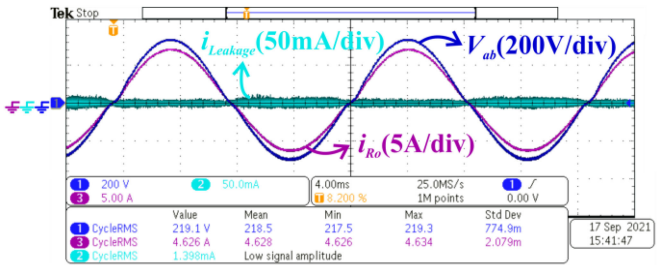



Fig. 17. Experimental output voltage, current in $R_o$ load, and leakage current of the experimental prototype of the inverter, operating at rated power condition.

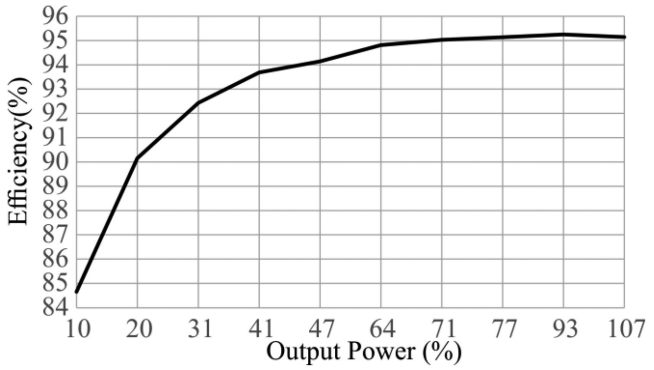



Fig. 18. Efficiency of the zeta inverter experimental prototype with purely resistive load.

Fig. 17 shows the leakage current along with the voltage and current in the load. This measurement is performed at rated power condition. It is observed that the leakage current has low amplitude, as expected, with its measured rms value equal to 1.4 mA.

Using the same power analyzer, data were collected to generate the efficiency curve, plotted in Fig. 18. According to this figure, when the output power is larger than 20% of the rated power, the measured efficiency ranges from 90% to 95.25%. A loss reduction design-oriented system would improve the converter efficiency.

## VII. Closed-Loop Control

Although the modeling and control of the proposed inverters is not the objective of this article, some simulation results will be presented in a summarized way, just to demonstrate that they can operate connected to the grid with current control.

Fig. 19 shows the inverter connected to the power grid, with block representation of the current control stage.

The dynamic behavior of the inverter is described by the set of differential equations

$$L_1\frac{di_{L1}}{dt} = -v_{C1}d + V_1(1-d) - i_{L1}(R_L + R_{DSon}) + i_{L2}R_{DSon} \tag{19}$$

$$L_2\frac{di_{L2}}{dt} = V_1 d - v_{C1}(1-d) - v_o + i_{L1}R_{DSon} - i_{L2}(R_L + R_{DSon}) \tag{20}$$

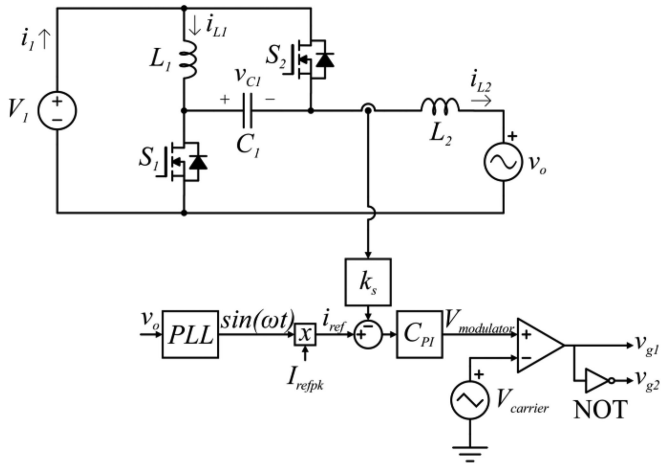



Fig. 19. Power and control stages of the inverter derived from the zeta converter connected to the grid.

$$C_1\frac{dv_{C1}}{dt} = i_{L1}d + i_{L2}(1-d). \tag{21}$$

The small signal transfer function $\tilde{i}_{L2}(s)/\tilde{d}(s)$, obtained for $\theta = 2\pi/3$, that is the critical angle from system stability point of view, is given by

$$\frac{\tilde{i}_{L2}(s)}{\tilde{d}(s)} = \frac{num_2 s^2 + num_1 s + num_0}{den_3 s^3 + den_2 s^2 + den_1 s + den_0} \tag{22}$$

where

$$num_2 = L_1C_1(V_1 + V_{C1}) \tag{23}$$

$$num_1 = L_1(1-D)(I_{L2} - I_{L1}) \tag{24}$$

$$num_0 = D(V_1 + V_{C1}) + R_{DSon}(I_{L2} - I_{L1}) \tag{25}$$

$$den_3 = L_1L_2C_1 \tag{26}$$

$$den_2 = C_1R_{DSon}(L_1 + L_2) \tag{27}$$

$$den_1 = L_1(1-D)^2 + L_2D^2 \tag{28}$$

$$den_0 = R_{DSon}. \tag{29}$$

Substituting the parameters of the power stage given in Table VI, with $R_L = R_{DSon} = 0.1\,\Omega$, we find

$$\frac{\tilde{i}_{L2}(s)}{\tilde{d}(s)} = \frac{6.945\times10^5 s^2 - 3.555\times10^9 s + 3.0048\times10^{13}}{s^3 + 173.4s^2 + 1.437\times10^8 s + 1.165\times10^{10}}. \tag{30}$$

A PI controller was employed, with a current sensor gain equal to $3\times10^{-4}$ and a PWM modulator gain equal to 1. The transfer function of the controller with these parameters is given by

$$C_{PI} = \frac{13.339(s+4788)}{s}. \tag{31}$$

The system shown in Fig. 19 was simulated. The grid voltage along with the current reference and the current in $L_2$ are shown in Fig. 20. It can be seen that the output current $i_{L2}$ follows the reference current $i_{ref}$ regardless the value of the phase angle $\theta$, which shows that the inverter operates with both positive and negative power flow.

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

TABLE VII
COMPARISON BETWEEN TRANSFORMERLESS COMMON-GROUND INVERTERS

| Transformerless Common-Ground Topology | Number of components | | | | Voltage | | | Output power | Switching frequency | Reported efficiency at rated power | Requires filter | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Switches | Diodes | Inductors | Capacitors | Input ($V_{DC}$) | Output ($V_{rms}$) | Max. semiconductor stress | | | | Input | Output |
| Proposed buck-boost | 4 | 0 | 1 | 0 | 400 | 220 | $V_1+V_{abpk}$ | 1 kW | 50 kHz | Theoretical: 94 % | Yes | Yes |
| Proposed SEPIC | 2 | 0 | 2 | 1 | 400 | 220 | $2V_1+V_{abpk}$ | 1 kW | 50 kHz | Theoretical: 95.6 % | Yes | Yes |
| Proposed zeta | 2 | 0 | 2 | 1 | 400 | 220 | $2V_1+V_{abpk}$ | 1 kW | 50 kHz | 95.25 % | Yes | No |
| Proposed boost-buck | 4 | 0 | 2 | 1 | 400 | 220 | $2V_1+V_{abpk}$ | 1 kW | 50 kHz | Theoretical: 95.5 % | No | No |
| Inverter in [6] | 5 | 0 | 1 | 0 | $\approx 100$ | 220 | $>V_{opk}$ | 200 W | 20 kHz | 92.5 % | Yes | Yes |
| Inverter in [15] | 5 | 3 | 1 | 0 | 92 | 100 | Not available | 168 W | 10 kHz | $\approx 87$ % | Yes | Yes |
| Inverter in [16] | 4 | 1 | 0 | 1 | 350 | 230 | $V_1$ | 1 kW | 24.4 kHz | 99.2 % | Yes | Yes |
| Inverter in [17] | 5 | 0 | 2 | 2 | 50 | 110 | $V_1+V_{abpk}$ | 300 VA | 50 kHz | $\approx 94$ % | No | No |
| Inverter in [18] | 5 | 0 | 0 | 1 | 400 | 220 | $V_1$ | 500 W | 20 kHz | $\approx 96.5$ % | Yes | Yes |
| Inverter in [19] | 4 | 2 | 0 | 2 | 400 | 220 | $2V_1$ | 500 W | 24 kHz | 97.4 % | Yes | Yes |
| Inverter in [20] | 5 | 1 | 1 | 1 | 340 | 220 | $2V_1$ | 1 kW | 100 kHz | 91.6 % | Yes | Yes |
| Inverter in [21] | 3 | 1 | 3 | 2 | 38 | 110 | $1.6V_{opk}$ [a] | 280 W | 40 kHz | 93 % | Yes | No |
| Inverter in [24] | 4 | 0 | 2 | 2 | 60 | 120 | $\approx 300$ V | 250 W | 50 kHz | Not available | No | Yes |
| Inverter in [29] | 8 | 1 | 0 | 2 | 200 | 240 | $2V_1$ | 1 kW | 20 kHz | 96 % | Yes | Yes |
| Inverter in [30] | 5 | 1 | 1 | 1 | 75 | $\approx 110$ | Not available | 300 W | 10 kHz | Not available | Yes | Yes |

[a]Only for $\alpha$ equal to 4.1.

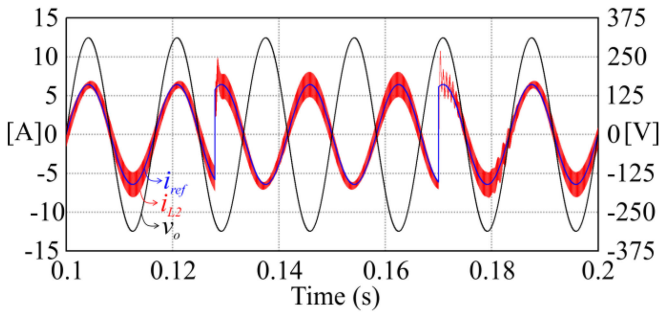



Fig. 20. Grid voltage, current reference, and $i_{L2}$ current of the grid-connected inverter.

## VIII. COMPARISON BETWEEN THE DERIVED TOPOLOGIES AND OTHER COMMON-GROUND INVERTERS

A comparison between the four inverters and other transformerless common-ground inverters, showing the number of components, voltage ratings, output power, switching frequency, reported efficiency at rated power, and the requirement for filter insertion, is presented in Table VII. Through this table, it is noted that each inverter has advantages and disadvantages when compared to other family members.

The inverter generated by the buck–boost converter does not need intermediate capacitors, in addition to subjecting the power semiconductors to a lower voltage stress, compared to the other three topologies.

The inverters generated by the SEPIC and zeta converters have the lowest number of switches, with only two power semiconductors. In addition, the inverter generated by the zeta converter does not need an output filter for connection to the power grid.

The inverter generated by the dc–dc boost–buck converter has the largest number of components among this family. However, it does not need the input and output filters. Except for this converter, only the one proposed in [17] does not require additional filters. It is to be noted that the number of power semiconductors is inversely proportional to the number of passive components.

The equations in Table II were used to calculate the expected efficiency for each inverter. It was considered the same switch used in the prototype. The theoretical results are presented in Table VII, except for the zeta inverter, which has an experimental result. However, the theoretical efficiency expected for this inverter was 96.2%.

It is observed that the efficiency of the proposed inverters is adequate, even with a nonoptimized design and component selection to increase efficiency.

It should also be noted that all obtained inverter topologies, as in conventional inverters, can generate or absorb reactive power when connected to the electrical grid, can operate as PWM rectifiers with unit power factor, active filters, and reactive power compensators, provided that appropriate current control is included. As for the input and output voltage specifications and range, the value of the dc input voltage must be larger than the peak value of the ac output voltage, as in a conventional full-bridge inverter.

## IX. CONCLUSION

A systematic method for generating common-grounded inverter topologies, used to obtain a family of inverters, was presented. The power stages of the generated topologies were

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.

dimensioned and the functioning of each one of them was verified by numerical simulation.

A comparative analysis between the generated topologies and other transformerless common-ground inverters has been presented. Given this comparison, the derived inverters appear to be suitable.

An experimental prototype of the inverter generated by the zeta bidirectional dc–dc converter was built and tested in the laboratory to verify the theoretical analysis. The maximum efficiency obtained with the nonoptimized experimental prototype was 95.25%.

It was demonstrated through experimentation and simulation that the inverter, in addition to processing active power, is also able to process reactive power. Therefore, it can be used to compensate reactive power, like the conventional inverter VSI full-bridge inverter.

Through computer simulation, it was also shown that the inverter with proper current control can interconnect a bidirectional dc voltage source with the grid, being able to operate with both positive and negative power flow.

The generated inverters are potential candidates for connection to the grid of small power photovoltaic generators and battery energy storage systems.

The presented methodology can be used to derive other inverter families from nonisolated bidirectional dc–dc converters.

## REFERENCES


[1] H. E. Murdock *et al.*, "Renewables 2020 global status report," REN21, Paris, France, 2020. Accessed: May 14, 2021. [Online]. Available: https://www.ren21.net/wp-content/uploads/2019/05/gsr_2020_full_report_en.pdf

[2] A. K. Raji and M. T. E. Kahn, "Investigation of common-mode voltage and ground leakage current of grid-connected transformerless PV inverter topology," *J. Energy Southern Afr.*, vol. 26, no. 1, pp. 20–24, Feb. 2015.

[3] C. A. Varghese, M. Karpagam, and T. Alwarsamy, "Analysis of leakage current and DC injection in transformerless PV inverter topologies," *Int. J. Eng. Technol.*, vol. 6, no. 1, pp. 453–459, Feb. 2014.

[4] L. Ma *et al.*, "Leakage current analysis of single-phase transformerless grid-connected PV inverters," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Yokohama, Japan, 2015, pp. 887–0892, doi: 10.1109/IECON.2015.7392211.

[5] S. Thomas, M. Stieneker, and R. W. De Doncker, "Development of a modular high-power converter system for battery energy storage systems," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Birmingham, U.K., 2011, pp. 1–10.

[6] M. Tofigh Azary, M. Sabahi, E. Babaei, and F. Abbasi Aghdam Meinagh, "Modified single-phase single-stage grid-tied flying inductor inverter with MPPT and suppressed leakage current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 221–231, Jan. 2018, doi: 10.1109/TIE.2017.2719610.

[7] B. Gu, J. Dominic, B. Chen, and J. Lai, "A high-efficiency single-phase bidirectional AC-DC converter with miniminized common mode voltages for battery energy storage systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, 2013, pp. 5145–5149, doi: 10.1109/ECCE.2013.6647396.

[8] M. Islam, S. Mekhilef, and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," *Renewable Sustain. Energy Rev.*, vol. 45, pp. 69–86, May 2015.

[9] R. Teodorescu, M. Liserre, and P. Rodriguez, "Photovoltaic inverter structures," in *Grid Converters for Photovoltaic and Wind Power Systems*, 1st ed., vol. 29. Chichester, U.K.: Wiley, 2011, ch. 2.

[10] M. Victor *et al.*, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic couse of direct current voltage, into a alternating current voltage," U.S. Patent 2005/0286281 A1, Dec. 2005.

[11] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007, doi: 10.1109/TPEL.2007.892120.

[12] H. Schmid *et al.*, "DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current," U.S. Patent 7 046 534 B2, May 2006.

[13] P. Knaup, "Inverter," International Patent Appl. WO 2007/048420 A1, May 2007.

[14] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005, doi: 10.1109/TIE.2005.847586.

[15] H. Patel and V. Agarwal, "A single-stage single-phase transformerless doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, Mar. 2009, doi: 10.1109/TEC.2008.2006551.

[16] Y. P. Siwakoti and F. Blaabjerg, "A novel flying capacitor transformerless inverter for single-phase grid connected solar photovoltaic system," in *Proc. IEEE 7th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2016, pp. 1–6, doi: 10.1109/PEDG.2016.7527086.

[17] V. Gautam and P. Sensarma, "Design of Ćuk-Derived transformerless common-grounded PV microinverter in CCM," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6245–6254, Aug. 2017, doi: 10.1109/TIE.2017.2677352.

[18] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013, doi: 10.1109/TPEL.2012.2203612.

[19] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5403–5415, Jul. 2017, doi: 10.1109/TIE.2016.2645162.

[20] S. U. Hasan, B. Shaffer, H. A. Hassan, M. J. Scott, Y. Siwakoti, and G. E. Town, "Common-ground transformerless inverter for solar photovoltaic module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018, pp. 167–172, doi: 10.1109/APEC.2018.8341004.

[21] A. Sarikhani, M. M. Takantape, and M. Hamzeh, "A transformerless common-ground three-switch single-phase inverter for photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8902–8909, Sep. 2020, doi: 10.1109/TPEL.2020.2971430.

[22] M. Chen and P. C. Loh, "A dual-boost H-bridge inverter with common ground for photovoltaic interfacing," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9515–9526, Oct. 2021, doi: 10.1109/TIE.2020.3026275.

[23] F. B. Grigoletto, "Multilevel common-ground transformerless inverter for photovoltaic applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 831–842, Feb. 2021, doi: 10.1109/JESTPE.2020.2979158.

[24] M. Verma, S. Gangavarapu, and A. K. Rathore, "Analysis and design of a novel Transformer-less-Inverter in grid-connected photovoltaic system," in *Proc. 14th IEEE Conf. Ind. Electron. Appl.*, Xi'an, China, 2019, pp. 79–84, doi: 10.1109/ICIEA.2019.8834150.

[25] L. Zhang, T. Zhu, L. Chen, and K. Sun, "A systematic topology generation method for dual-buck inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6, doi: 10.1109/ECCE.2016.7854795.

[26] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4537–4551, Jul. 2015, doi: 10.1109/TIE.2015.2399278.

[27] D. Cao, S. Jiang, X. Yu, and F. Z. Peng, "Low-cost single-phase semi-Z-source inverter," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 429–436, doi: 10.1109/APEC.2011.5744632.

[28] N. Vázquez, M. Rosas, C. Hernández, E. Vázquez, and F. J. Perez-Pinal, "A new common-mode transformerless photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6381–6391, Oct. 2015, doi: 10.1109/TIE.2015.2426146.

[29] B. Shaffer, H. A. Hassan, M. J. Scott, S. U. Hasan, G. E. Town, and Y. Siwakoti, "A common-ground single-phase five-level transformerless boost inverter for photovoltaic applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 368–374, doi: 10.1109/APEC.2018.8341037.

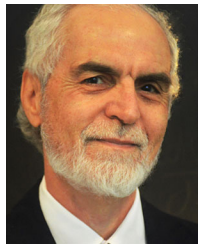
[30] P. K. Chamarthi, M. Shawky El Moursi, V. Khadkikar, and K. H. Al Hosani, "A novel single-stage buck-boost transformerless inverter for 1-$\phi$ grid-connected solar PV systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 3341–3345, doi: 10.1109/APEC39645.2020.9124142.


Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.



**Gabriel de O. Assunção** (Student Member, IEEE) was born in Londrina, Brazil, in 1988. He received the B.S. degree in electronic engineering and the M.S. degree in electrical engineering from the Federal University of Technology – Paraná, Ponta Grossa, Brazil, in 2013 and 2016, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the Federal University of Santa Catarina, Florianopolis, Brazil.

His research interests include power electronics, rectifiers, inverters, power converters for storage systems, and renewable energy sources.



**Ivo Barbi** (Life Fellow, IEEE) was born in Gaspar, Brazil. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr. Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society, the Brazilian Power Electronics Conference, in 1990, and the Brazilian Institute of Power Electronics and Renewable Energy, in 2016. He is currently a Researcher with the Solar Energy Research Center, Florianópolis, SC, Brazil, and a Professor Emeritus of electrical engineering with UFSC.

Dr. Barbi was a recipient of the 2020 IEEE William E. Newell Power Electronics Award. He was an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS for several years.

Authorized licensed use limited to: UNIVERSIDADE FEDERAL DE SANTA CATARINA. Downloaded on June 11,2022 at 12:44:03 UTC from IEEE Xplore. Restrictions apply.